Synchro/Resolver-Digital Converter
(HSDC/HRDC27 Series)

1. Features (see Fig. 1 for outside view, and Table 1 for models)

- Resolution: 12 bits, 14 bits
- High tracking speed
- Hybrid integration, metal case
- Three-state latch output
- With velocity signal Vel output
- Indefinite compatibility with AD1740 series

Size : 45.39×29. 0×7.2mm³
Weight: 26g

Fig. 1 Outside view of HSDC/HRDC27 series

Table 1 Product models

12-bit		14-bit	
Synchro	Resolver	Synchro	Resolver
HSDC2742－412	HRDC2742－414	HSDC2754－612	HRDC2754－414
	HRDC2742－418		HRDC2754－418
	HRDC2742－618		HRDC2754－618
			HRDC2754－666
			HRDC2754－614

2. Scope of application

Servo system; antenna system; angle measurement; simulation technology; cannon control; control of industrial machine tools

3. Description

HSDC/HRDC27 series is the digital-to-synchro/resolver converter for continuous tracking of type II servo loop, it parallelly latches and outputs 12-bit or 14-bit natural binary coded data with 32-line dual-in-line metal package, features the advantages of small volume, light weight and high reliability etc., it is widely applied in such automatic control system as Radar system, navigation system, etc.

The operating power adopts ±15V and + 5V DC power. There are two types of output signal: three-line synchro and reference signal (SDC converter) or four-line resolver and reference signal (RDC converter); the output adopts parallel digital codes of binary system.

Table 2 Rated conditions and recommended operating conditions

Absolute max. rated value	Supply voltage Vs: ± 17.5V Logical voltage V_L: +5.5V Storage temperature range: -55℃~+125℃
Recommended operating conditions	Supply voltage Vs: ± 5V Logical voltage V_L: 5V Effective value of reference voltage V_{Ref}: ±10% of nominal value Validity of signal voltage V_1*: ±5% of nominal value Reference frequency f*: 50Hz~2.6kHz Operating temperature range T_A: -40~+85℃，-55~+105℃

Note: * indicates it can be customized as per user's requirement.

This series is a digital converter of modular structure for synchro resolver with built-in solid-state SCOTT isolation converter, designed according to the principle of Model II servo, and can realize continuous tracking and conversion.

Differential isolation input and data output is three-state latch mode, suitable for analog signal/digital signal conversion of three-wire type synchro and four-wire resolver. With fast conversion speed and stable and reliable performance, this device can be widely applied in angle measurement and automatic control system.

This product is made by the thick-film hybrid integration process and is 32-wire DIP totally sealed metal package. Both the design and manufacture of the product satisfy the requirements of GJB2438A-2002 "General specification for packages of hybrid integrated circuits" and specific specification of the product.

4. Electrical performance (Table 2, Table 3)

Table 3 Electric characteristics

Parameter		HSDC/HRDC2742 Enterprise military standard(Q/HW30859-2006)	HSDC/HRDC2754 Enterprise military standard(Q/HW30859-2006)	Unit	Remarks
Converter Performance	Precision	±8.5	±5.3	Angular minute	
	tracking speed	25(min)	12(min)	rps	@400 Hz excitation
	resolution	12	14	bit	
Signal and reference frequency		50～2 600	50～2 600	Hz	optional *
Signal input voltage		11.8, 26, 90	11.8, 26, 90	V	optional * *
Reference input voltage		11.8, 26, 115	11.8, 26, 115	V	optional * *
Step response		100	150	ms	
Accelerantion constant		82 000	39 000	s^{-2}	
Power consumption		0.86max	1.3max	W	
Busy pulse width		1max	1max	μs	
Digital output loading capacity		2max	2max	TTL	

Note: * For converters with frequency of 50kHz, 2kHz and others, the dynamic parameters are different, and they can be provided as per customers' requirements;

**: Customization is available.

5. Operating principle

The synchro input signal (or input signal of resolver) is converted into the orthogonal signal through internal differential isolation:

$$V_1 = KE_0 \sin\theta \sin\omega t,\ V_2 = KE_0 \cos\theta \sin\omega t$$

Where, θ is analog input angle

The digital angle φ of internal reversible counter of these two signals are multiplied in the multiplier of Sine and Cosine functions and are error treated:

$$KE_0 \sin\theta \cos\varphi \sin\omega t - KE_0 \cos\theta \sin\varphi \sin\omega t = KE_0 \sin(\theta - \varphi)\sin\omega t$$

The signals are sent to voltage controlled oscillator after amplification, phase discrimination and integration filtration, if θ-φ≠0, the voltage controlled oscillator will output pulse to change the data in the reversible counter, till θ-φ becomes zero within the accuracy of the converter, during this process, the conversion tracks the change of input angle θ all the time.

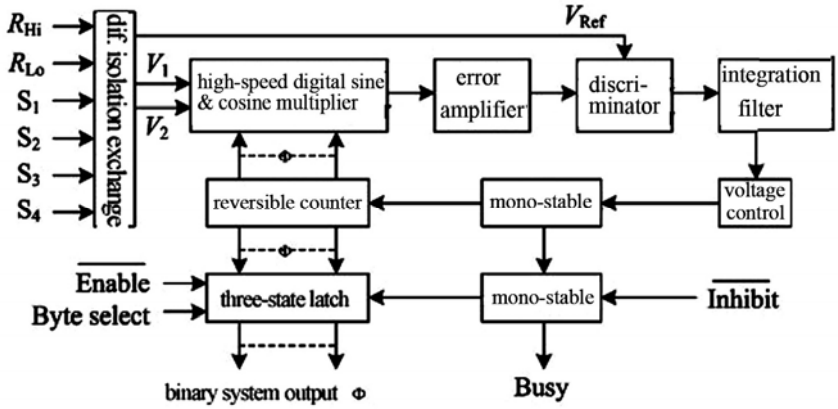
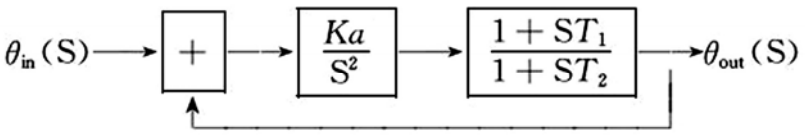


Fig.2 Block diagram of operating principle

transfer function of converter



closed-loop function

$$\frac{\theta_{out}(S)}{\theta_{in}(S)} = \frac{1 + T_1 S}{1 + ST_1 + S^2/Ka + S^3 T_2/Ka}$$

Methods of data transfer and time sequence

There are two methods for reading out the valid data of converter:

(1) Inhibit method (synchronous reading):

A: the converter is connected to 16-bit bus. Byse 1 is connected to logic "1".

$\overline{\text{Inhibit}}$ is set to logic "0" from logic "1" (data locking), wait for 1μs; set $\overline{\text{Enable}}$ to logic "0", the latch data inside the converter is allowed to be output; read 12-bit or 14-bit data; set **Inhibit** to logic "1" so as to get ready for reading next valid data (see the time sequence diagram of 16-bit transfer).

B: the converter is connected to 8-bit bus, D_1~D_8 bit are connected to data bus, and the rest are empty.

$\overline{\text{Inhibit}}$ is set to logic "0" from logic "1" (data locking), wait for 1μs; set **Enable** to logic "0", the latch data inside the converter is allowed to be output; if Byse1 is set to logic "1", the converter directly reads the higher 8-bit data, if Byse1 is set to logic "0", the converter reads the rest bits, automatically adds zero for incomplete bits; set $\overline{\text{Inhibit}}$ to logic "1" in order to get ready for reading next valid data (see Fig. 3 and Fig. 4 for 8-bit transfer time sequence).

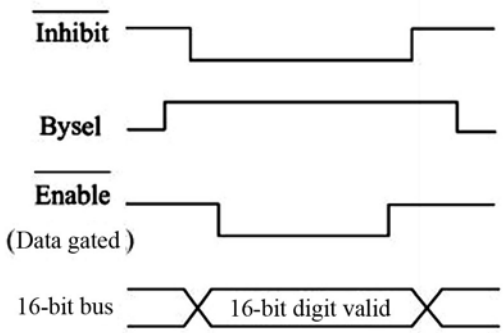


Fig. 3 Time sequence chart for 16-bit bus transfer

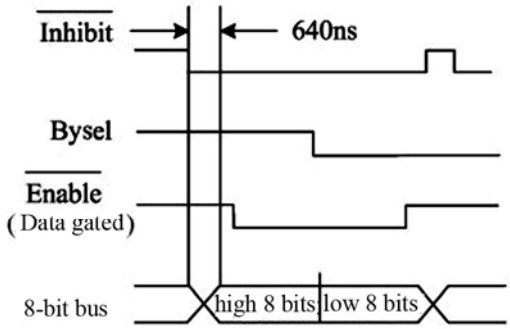


Fig. 4 Time sequence chart for 8-bit bus transfer

(2) Busy method (asynchronous reading):

In asynchronous reading mode, $\overline{\text{Inhibit}}$ is set to logic "1" or empty, whether the internal loop is always in the stable state or whether the output data is valid shall be determined through the state of busy signal **Busy**. When Busy signal is at high level, it indicates the data is being converted, and the data at this time is unstable and invalid; when Busy signal is at low level, it indicates the data conversion has been completed, and the data at this time is stable and valid. Once high level occurs in Busy during reading, the reading of this time is invalid. In asynchronous reading mode, Busy output is pulse train of TTL level, the width between is related to rotational speed. Likewise, there are also 8-bit and 16-bit two use methods of bus, at the time of valid data output, data reading is also controlled by $\overline{\text{Enable}}$, refer to time sequence diagram of data transfer (Fig.5 and Fig.6)

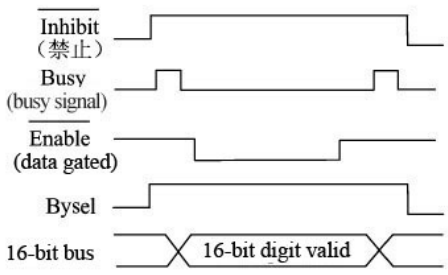


Fig. 5 Time sequence of 16-bit bus transfer

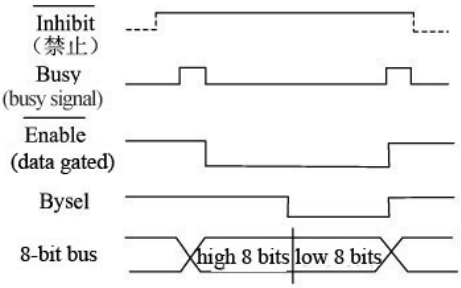


Fig. 6 Time sequence of 8-bit bus transfer

6 MTBF Curve (Fig.7)

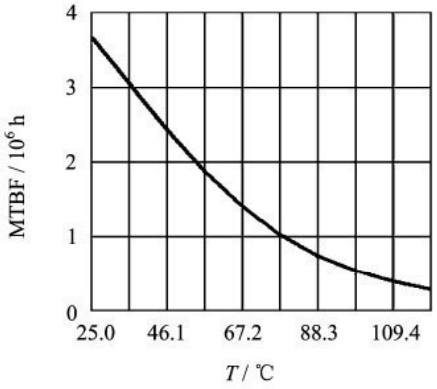


Fig.7 MTBF-Temperature Curve
(note: as per GJB/Z299B-98, envisaged good ground condition)

7 Pin designation (Fig.8, Table 3)

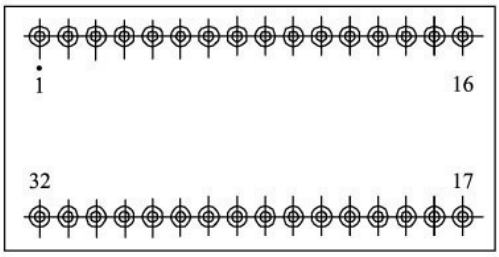


Fig. 8 Pinouts (bottom view)

Table 3 Function description of pins

pin	Symbol	Function	pin	Symbol	Function
1～14	$D_1 \sim D_{14}$	digital output	24	Bysel	bit selection
15	R_{Lo}	excitation signal input	25	NC	leave unconnected
16	R_{Hi}	excitation signal input	26	$\overline{\text{Enable}}$	data gated
17	S_4	signal input	27	Busy	busy pulse output
18	S_3	signal input	28	$\overline{\text{Inhibit}}$	data latch control
19	S_2	signal input	29	+15V	power supply
20	S_1	signal input	30	GND	power supply ground
21	NC	leave unconnected	31	−15V	power supply
22	Vel	velocity voltage output	32	+5V	power supply
23	Case	shell ground			

Notes:

① For 12-bit converter, pin 13 and 14 are left unconnected.

② For SDC converter, pin 17 is left unconnected.

③ Power supply: ±15V, +5V, GND, the power shall not be connected reversely, otherwise, components will be damaged.

④ Binary digital output: 12 bits and 14 bits, respectively.

⑤ R_{Hi}, R_{Lo}: excitation signal input.

⑥ S_1, S_2, S_3 and S_4: signal input of synchro or resolver.(S_4 not used for the synchro)

⑦ Busy: busy signal

This signal indicates whether the binary number output from the converter is valid or not. When Busy is at

high level, it indicates the converter is carrying out data conversion, the data output at this time is invalid; when Busy is at low level, the data in the converter is stable and the data output at this time is valid.

⑧ $\overline{\text{Enable}}$ Data gating

This pin is the input pin of control logic, its function is to output data to the converter to realize three-state control. Low level is valid, the output data of converter occupies the data bus. When it is at high level, the data output pin of converter is in three states, the device does not occupy the bus.

⑨ $\overline{\text{Inhibit}}$ data locking control (Inhibit signal)

This pin is the input pin of control logic, its function is to output data externally to the converter to realize optional latching or bypass control.

At high level, the output data of the converter directly outputs without latching; at low level, the output data of the converter is latched, the data is not updated, but the internal loop is not interrupted, and tracking is working all the time. $\overline{\text{Inhibit}}$ has connected high resistance (whether the device adopts data bus to output the data depends on the state of $\overline{\text{Enable}}$).

⑩ Byse1: bit selection terminal

This is a control terminal specially designed for connecting the converter with 8-bit data or 16-bit data bus. When the converter is connected with 16-bit data bus, Byse1 is pulled up internally, the converter can directly output 12-bit or 14-bit data; when the converter is connected with 8-bit data bus, Byse1 is at a high level, the converter outputs data of higher 8 bits (D_1~D_8), when Byse1 is at low level, the converter outputs data of the rest bits (copying the data of the rest bits to bit D_1~D_8), and automatically fills zero for the data of short bits. It shall be noted that it is only needed to connect D_1~D_8 when the converter is connected with 8-bit data bus, other data pins are left unconnected.

8 Table of weight values

Table 4 Table of weight values

bit number	angle	bit number	angle	bit number	angle
1(MSB)	180.000 0	6	5.625 0	11	0.175 8
2	90.000	7	2.812 5	12(for 12-bit LSB)	0.087 9
3	45.000	8	1.406 3	13	0.043 9
4	22.500 0	9	0.703 1	14(for 14-bit LSB)	0.022 0
5	11.250 0	10	0.351 6		

9 Connection diagram for typical application (Fig. 9)

Besides being directly used in precise measurement of rotational angle of the synchro or resolver, the shaft angle converter can also constitute two-speed measurement system or other digital measurement control system of higher precision. Fig.9 is an example of two-speed system composed of the converter. The two-speed system established on the principle of combination of coarse and precise measurement has a higher conversion precision, Fig.9 shows the two-speed conversion system composed of two synchros (or resolvers) coupled through the gearbox, two SDC converters and a two-speed processor HTSL19, its output reaches 19 bits.

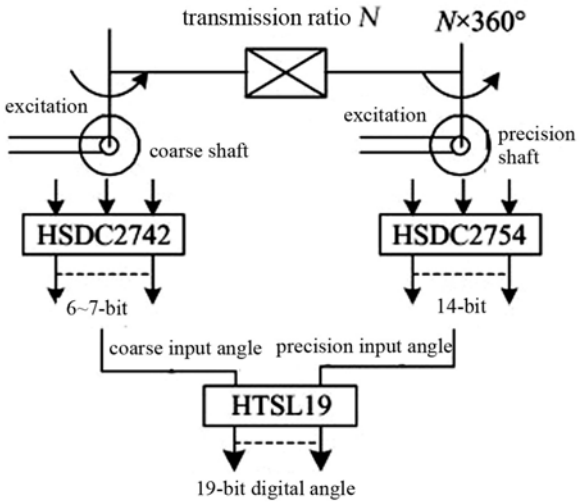


Fig. 9 Application of SDC Two-Speed System

10 Package specifications (unit: mm) (Fig.10)

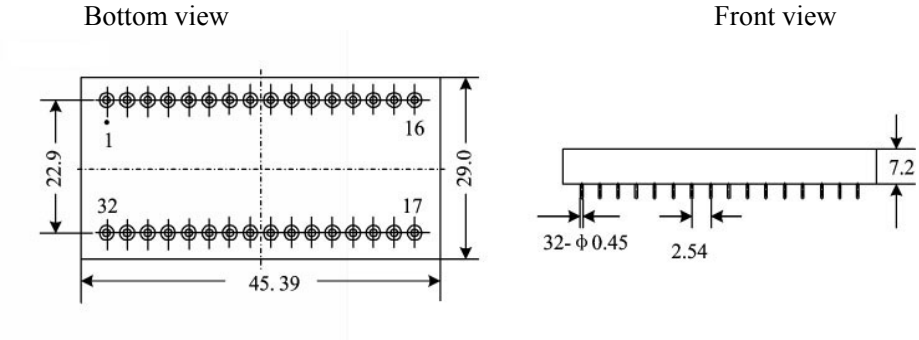


Fig.10 Outside view of package

Table 5 Case materials

Case model	Header	Header plating	Cover	Covering plating	Pin material	Pin plating	Sealing style	Notes
UP4529-32a	Kovar (4J29)	Au	Iron/ nickel alloy (4J42)	Au	Kovar (4J29)	Au	Matched seal	Plating of pin 23 is Au

11 Part numbering key (Fig. 11)

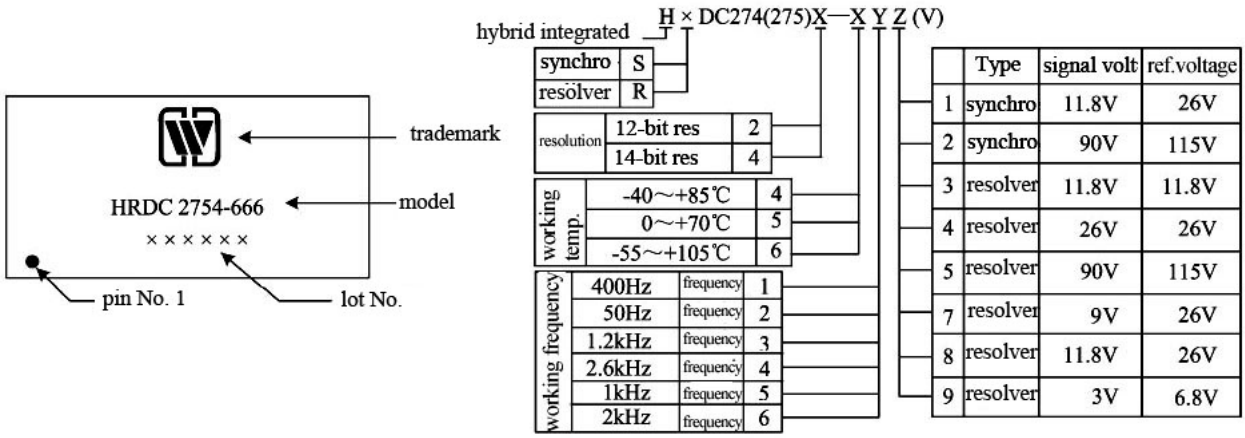


Fig. 11 Park numbering key

Note: if above signal voltages and reference voltages(Z) are non-standard, they shall be given as follows:

H ×DC 274(275)× — XYZ — ×/×

same as above

reference voltage +/ signal voltage

(e.g. reference voltage 5V and signal voltage 3V are expressed as -5/3)

Application notes:

- ✧ Supply the power correctly, upon power-on, be sure to correctly connect the positive and negative pole of the power supply for fear of burning.
- ✧ Connection of the converter

  ±15V, +5V and GND shall be connected to corresponding pins on the converter, notice that the polarities of the power supply must be correct, otherwise, components may be damaged. It is recommended to connect 0.1μF and 6.8μF bypass capacitance in parallel between each power supply terminal and ground. Signal and excitation source are allowed to be connected to S_1, S_2, S_3 and S_4 and R_{Hi} and R_{Lo} within an error of 5%. It is only needed to connect D_1~D_8 when the converter is connected with 8-bit data bus, other data pins are left unconnected.

  When the converter is connected to 16-bit data bus, D_1~D_{14} or (D_1~D_{12}) shall all be connected.

  The signal input shall match the phase of the excitation so that they can be correctly connected with the converter, their phases are as follows:

$$R_{Hi} \sim R_{Lo} : V_R \sin \omega t$$

For the synchro:

$$S_1 \sim S_3 \; is : E_{S_1 \sim S_3} = E_{R_{Lo} \sim R_{Hi}} \sin\theta \sin \omega t$$

$$S_3 \sim S_2 \; is : E_{S_3 \sim S_2} = E_{R_{Lo} \sim R_{Hi}} \sin(\theta + 120^\circ) \sin \omega t$$

$$S_2 \sim S_1 \; is : E_{S_2 \sim S_1} = E_{R_{Lo} \sim R_{Hi}} \sin(\theta + 240^\circ) \sin \omega t$$

For the resolver:

$$S_1 \sim S_3 \; is : E_{S_1 \sim S_3} = E_{R_{Lo} \sim R_{Hi}} \sin\theta \sin \omega t$$

$$S_2 \sim S_4 \; is : E_{S_2 \sim S_4} = E_{R_{Hi} \sim R_{Lo}} \cos(\theta \sin \omega t$$

- ✧ Upon assembly, the bottom of the product shall fit to the circuit board closely so as to avoid damage of pins, and shockproof provision shall be added, if necessary.
- ✧ When the user places an order for the product, detailed electric performance indexes shall refer to the relevant enterprise standard.