Synchro/Resolver-Digital Converter (HSDC/HRDC211 Series)

1 Features (see Fig. 1 for outside view, and Table 1 for models)

- Excitation frequency 50Hz, 400Hz and 2.6kHz
- Resolution: 10 bits, 12 bits, 14 bits
- High tracking speed
- Non-standard input is adjustable through external resistance or adjusted at the product input terminal
- DC voltage output directly proportional to angular velocity
- Compatible with SDC1700 series of American AD company

Size: 79.4×66.7×11.3mm³
Weight: 108g

Fig. 1 Outside view of HSDS/HRDC211 series

Table 1 Product models

12-bit		14-bit	
Synchro	Resolver	Synchro	Resolver
HSDC2112-412	HRDC2112-418	HSDC2114-412	HRDC2114-418
HSDC2112-411	HRDC2112-414	HSDC2114-422	HRDC2114-414
	HRDC2112N	HSDC2114-411	HRDC2114N

2 Scope of application

Servo system; antenna system; angle measurement; simulation technology; cannon control; control of industrial machine tools

3 Description

HSDC/HRDS211 series is a digital converter of modular structure for synchro/resolver with built-in solid-state SCOTT isolation converter, designed according to the principle of type II servo, and can realize continuous tracking and conversion.

The operating power is ±15V and + 5V DC power. There are two types of output signal: three-line synchro and reference signal (SDC converter) or four-line resolver and reference signal (RDC converter); the output is parallel digital codes of binary system.

4 Electrical performance (Table 2, Table 3)

Table 2 Rated conditions and recommended operating conditions

Absolute max. rated value	Supply voltage Vs: ± 17.5V
	Logical voltage V_L: +7V
	Storage temperature range: -55℃~105℃
Recommended operating conditions	Supply voltage Vs: ±15V
	5V logic supply voltage V_L: +5V
	Effective value of reference voltage V_{Ref}: 11.8V, 26V, 115V
	Effective value of reference voltage V_1*: 11.8V, 26V, 90V
	Reference frequency f*: 50Hz, 400Hz, 2.6kHz
	Operating temperature range T_A: 0~70℃, -40~+85℃

Note: * indicates it can be customized as per user's requirement.

5 Operating principle

The synchro input signal (or input signal of resolver) is converted into the orthogonal signal through internal differential isolation:

$$V_1 = KE_0 \sin\theta \sin\omega t \ , \ V_2 = KE_0 \cos\theta \sin\omega t$$

Table 3 Electric characteristics

Parameter		Conditions	HRDC/HSDC2110	HRDS/HSDC2112	HRDC/HSDC2114	Unit	Notes
Precision		±10% signal and reference voltage fluctuation ±10% operating frequency fluctuation ±5% power supply fluctuation	±22	±8.5	±5.3	Angular minute	
Tracking velocity		—	5(50Hz) 36(400Hz) 75(2.6kHz)	5(50Hz) 36(400Hz) 75(2.6kHz)	1.38(50Hz) 12(400Hz) 25(2.6kHz)	Rev/sec	
Resolution		binary system and digital code	10	12	14	bit	
Signal and ref. frequency		—		500, 400, 2.6k		Hz	Optional
Effective value of signal input voltage		—		11.8, 26, 90		V	Optional
Effective value of reference input voltage		—		11.8, 26, 115		V	Optional
signal input impedance	90V signal single end	—		100		kΩ	
	90V signal differential	—		200		kΩ	
	26V signal single end	—		28		kΩ	
	26V signal differential	—		56		kΩ	
	11.8V signal single end	—		13		kΩ	
	11.8V signal differential	—		26		kΩ	
ref. input impedance	115V ref. single end	—		127		kΩ	
	115V ref. differential	—		254		kΩ	
	26V ref. single end	—		28		kΩ	
	26V ref. differential	—		56		kΩ	
	11.8V ref. single end	—		13		kΩ	
	11.8V ref. differential	—		26		kΩ	
step response		50Hz		1 500max		ms	
		400Hz		125max			
		2.6kHz		75max			
power	$+V_s=+15V$	—		18		mA	
power	$-V_s=+15V$	—		18			
	$V_L=+5V$	—		2			
busy signal	pulse width	—		200～600		ns	
	load capacity	—		3max		TTL	
digital output	V_{OH}	—		2.4min		V	
	V_{OL}	—		0.4max		V	
	load capacity	—		3max		TTL	

Where, θ is analog input angle

The orthogonal signal is multiplied by the binary digital angle φ in the internal reversible counter in the sine-cosine function multiplier and an error function is obtained:

$$KE_0 \sin\theta\cos\varphi\sin\omega t - KE_0\cos\theta\sin\varphi\sin\omega t = KE_0 \sin(\theta-\varphi) \sin\omega t$$

The signals are sent to voltage controlled oscillator after amplification, phase discrimination and integration filtration, if θ-φ≠0, the voltage controlled oscillator will output pulse to change the data in the reversible counter, till θ-φ becomes zero within the accuracy of the converter, during this process, the converter tracks the change of input angle θ all the time. For working principle, see Fig. 2.

Transfer function: following are parameters for transfer function of HSDC2112 and HSDC2114(400Hz), for other models, please contact the manufacturer directly.

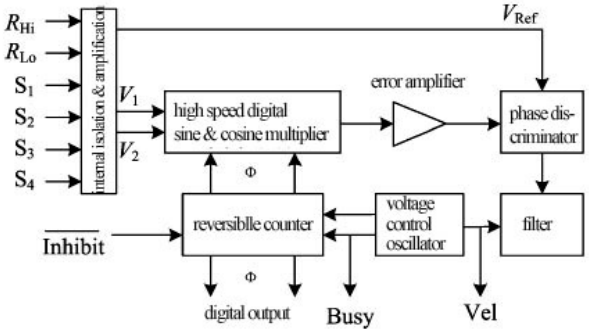


Fig.2 Block diagram for operating principle of the converter

HSDC2112(400Hz)

$$\theta_{out}(S)/\theta_{in}(S) = \frac{8.8\times10^{7}(1+6.8\times10^{-3}S)}{S^{3}+8.04\times10^{2}S^{2}+6.1\times10^{5}S+8.8\times10^{7}}$$

HSDC2114(400Hz)

$$\theta_{out}(S)/\theta_{in}(S) = \frac{2.95\times10^{7}(1+8.2\times10^{-3}S)}{S^{3}+8.05\times10^{2}S^{2}+1.95\times10^{5}S+2.95\times10^{7}}$$

(1) Data transfer

There are two methods for reading out the valid data of converter as follows:

$\overline{\text{Inhibit}}$ method (synchronous reading):

Set $\overline{\text{Inhibit}}$ to logic "0", at this time, the converter will stop tracking. Wait for 1μs till the output data is stable, read the data, the data read is the valid one at this time (1μs has been delayed).Set $\overline{\text{Inhibit}}$ to logic "1", at this time, the converter will start tracking again in order to get ready for reading next valid data.

Busy method (asynchronous reading):

In asynchronous reading mode, $\overline{\text{Inhibit}}$ is set to logic "1" or vacant, if the internal loop is always in stable state or if the output data is valid shall be determined through the state of busy signal Busy. When Busy signal is at high level, it indicates the data is being converted, and the data at this time is unstable and invalid; when Busy signal is at low level, it indicates the data conversion has been completed, and the data at this time is stable and valid. In asynchronous reading mode, Busy output is pulse train of TTL level, the width between is related to rotational speed. Refer to time sequence diagram of data transfer Fig. 3.

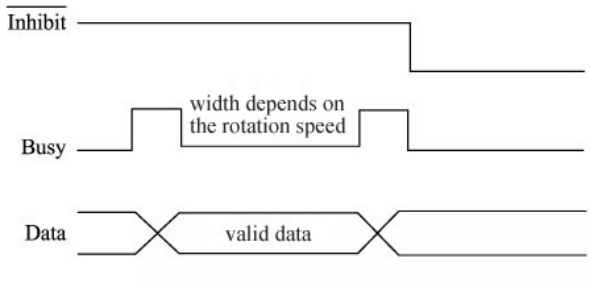


Fig.3 Time sequence of data transfer

(2) Attenuation method of input signal

If the synchro or resolver the user used is non-standard, in order to make the input signal voltage and input excitation voltage match the nominal values of the converter, the user may adopt the method of external attenuation resistance connected in series, i.e. for every 1V exceeding the nominal value, connect 1.1kΩ resistance in series at the corresponding input terminal. When using the converter, the series resistance at each terminal shall be precisely selected and furnished, and resistance material of the same lot shall be adopted so as to ensure the conversion accuracy of the converter within the wide temperature range, for every 0.1% the matching error of the series resistance will generate 1.7 angular minute conversion error.

It is recommended by the manufacturer that it is preferable to notify the manufacturer to customize the non-standard synchro or resolver as per the required parameters when the user uses them.

6 MTBF curve (Fig. 4)

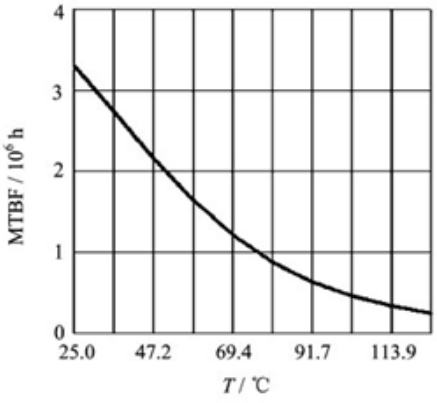
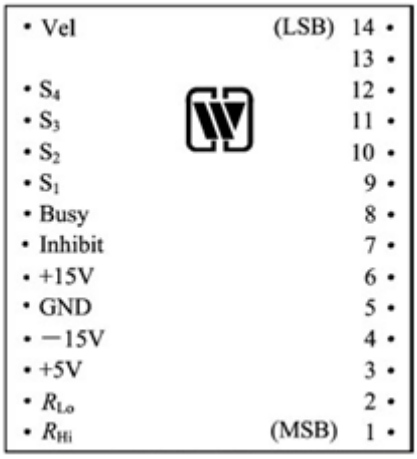


Fig. 4 MTBF-temperature curve (Note: according to GJB/Z299B-98, envisaged good ground condition)

7 Pin designation (Fig. 5, Table 4)



Notes:

① the above structure is suitable for HRDC2114

② for SDC, no pin S_4

③ for 12-bit device, no pin 13 and 14, for 10-bit device, no pin 11, 12, 13 and 14.

Fig.5 Pin designation (Top view)

Table 4 Pin designation

Pin	Symbol	Function	Pin	Symbol	Function
1	D_1	Digital output of bit 1 (MSB)	15	Vel	Angular velocity voltage output
2	D_2	Digital output of bit 2	16	S_4	Signal input
3	D_3	Digital output of bit 3	17	S_3	Signal input
4	D_4	Digital output of bit 4	18	S_2	Signal input
5	D_5	Digital output of bit 5	19	S_1	Signal input
6	D_6	Digital output of bit 6	20	Busy	Busy signal input
7	D_7	Digital output of bit 7	21	$\overline{\text{Inhibit}}$	Inhibit signal input
8	D_8	Digital output of bit 8	22	+15V	+15V Power supply
9	D_9	Digital output of bit 9	23	GND	Ground
10	D_{10}	Digital output of bit 10 (10-bit LSB)	24	-15V	-15V Power supply
11	D_{11}	Digital output of bit 11	25	+5V	+5V Power supply
12	D_{12}	Digital output of bit 12 (10-bit LSB)	26	R_{Lo}	Low end of reference signal input
13	D_{13}	Digital output of bit 13	27	R_{Hi}	High end of reference signal input
14	D_{14}	Digital output of bit 14 (10-bit LSB)			

Notes:

① Power supply: ± 15V, +5V, GND

② Binary digital output: 10 bits, 12 bits and 14 bits, respectively.

③ R_{Hi}, R_{Lo}: excitation signal input.

④ S_1, S_2, S_3 and S_4: signal input of synchro or resolver.(S_4 not used for the synchro)

⑤ Vel: velocity signal. It is a voltage signal, the value of which is proportional to the angular rotational speed of the shaft.

⑥ Busy: busy signal. It indicates if the converter data is being in the updating state. When Busy is at high level, it indicates the converter is carrying out data conversion, the data output at this time is invalid; when Busy is at low level, the data in the converter is stable and the data output at this time is valid.

⑦ $\overline{\text{Inhibit}}$: This is an external inhibit signal. By this signal, the internal tracking status can be controlled, when it is logic "1", the converter is in normal tracking status inside, at this time, Busy signal indicates whether the output data is valid or not, when Inhibit is logic "0", the converter stops tracking the status temporarily, the output data remains stable and is the valid output data. When Inhibit is logic "1", the converter will start tracking again (the maximum recovery time is approximately equal to the maximum step

response time). This pin has been pulled up inside.

8 Table of weight values (Table 5)

Table 5 Table of weight values

Bit	Angle	Bit	Angle	Bit	Angle
1(MSB)	180.000 0	6	5.625 0	11	0.175 8
2	90.000 0	7	2.812 5	12 (for 12-bit LSB)	0.087 9
3	45.000 0	8	1.406 3	13	0.043 9
4	22.500 0	9	0.703 1	14(for 14-bit LSB)	0.022 0
5	11.250 0	10 (for 10-bit LSB)	0.351 6		

9 Connection diagram for typical application (Fig. 6)

(1) Connection of the converter

±15V, +5V and GND shall be connected to corresponding pins on the converter, notice that the polarities of the power supply must be correct, otherwise, the converter may be damaged. It is recommended to connect 0.1μF and 6.8μF bypass capacitance in parallel between each power supply terminal and ground.

Signal and excitation source are allowed to be connected to S_1, S_2, S_3 and S_4 and R_{Hi} and R_{Lo} terminal within an error of 5%.

The signal input shall match the phase of the excitation source so that they can be correctly connected with the converter, their phases are as follows:

$$R_{Hi} \sim R_{Lo} : V_R \sin \omega t$$

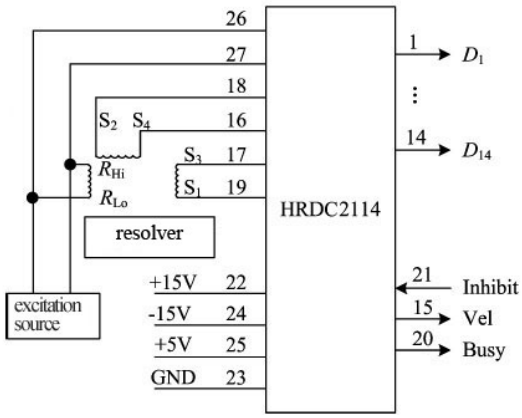


Fig.6 Connecting diagram of typical application

For the synchro, signal inputs are:

$$For\ S_1 \sim S_3 : E_{S_1 \sim S_3} = E_{R_{L0} \sim R_{Hi}} \sin\theta \sin\omega t$$

$$For\ S_3 \sim S_2 : E_{S_3 \sim S_2} = E_{R_{L0} \sim R_{Hi}} \sin(\theta + 120°) \sin\omega t$$

$$For\ S_2 \sim S_1 : E_{S_2 \sim S_1} = E_{R_{L0} \sim R_{Hi}} \sin(\theta + 240°) \sin\omega t$$

For the resolver:

$$For\ S_1 \sim S_3 : E_{S_1 \sim S_3} = E_{R_{L0} \sim R_{Hi}} \sin\theta \sin\omega t$$

$$For\ S_2 \sim S_4 : E_{S_2 \sim S_4} = E_{R_{Hi} \sim R_{Lo}} \cos\theta \sin\omega t$$

Note: no input signal of R_{Hi}, R_{Lo}, S_1, S_2, S_3 and S_4 is not allowed to be connected to other pins for fear of damage of the device.

(2) Interface with computer

In order to prevent data collection during high level of the Busy pulse and to ensure to acquire valid data, connection in Fig.7 can be adopted:

(3) Application of the converter

Besides being directly used in precise measurement of rotational angle of the synchro or resolver, the shaft angle converter can also constitute two-speed measurement system or other digital measurement control system of higher precision.

Fig. 8 is an example of two-speed system composed of the converter. The two-speed system established on the principle of combination of coarse and precise measurement has a higher conversion precision, the figure shows the two-speed conversion system composed of two synchros (or resolvers) coupled through the gearbox, two SDC converters and a two-speed processor HTSL19, its output reaches 19 bits.

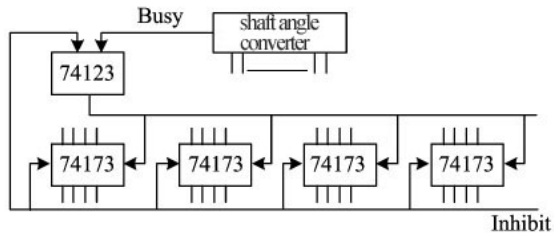


Fig.7 A feasible external computer interface circuit

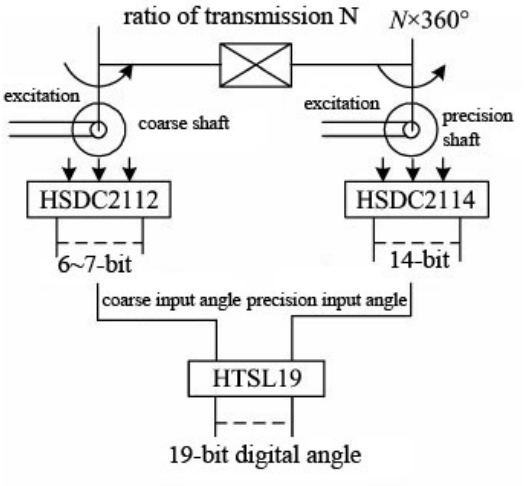


Fig.8 Application of two-speed system of SDC

Fig.9 shows a digital control servo system. It utilizes the negative feedback loop of digital control constituted by SDC to achieve precision control of the rotational angle.

10 External dimensions and description of package (unit: mm) (Fig.10)

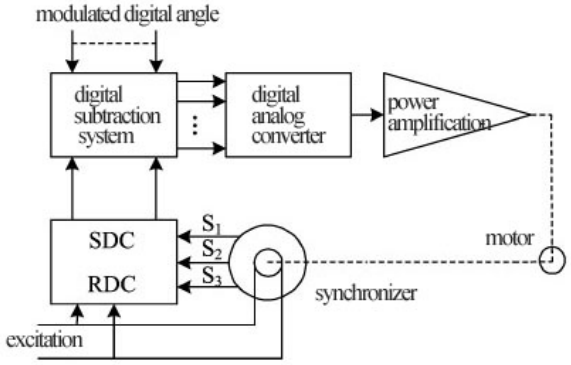


Fig.9 Digital control servo system

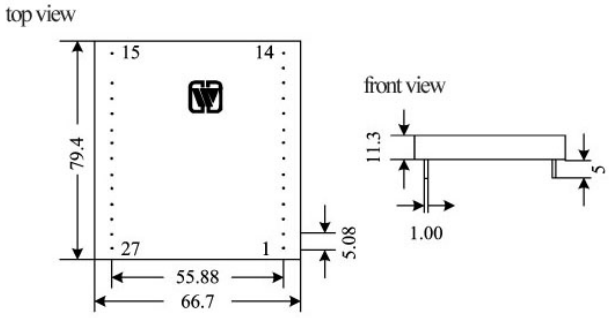


Fig.10 Outside view of package

11 Part numbering key (Fig. 11)

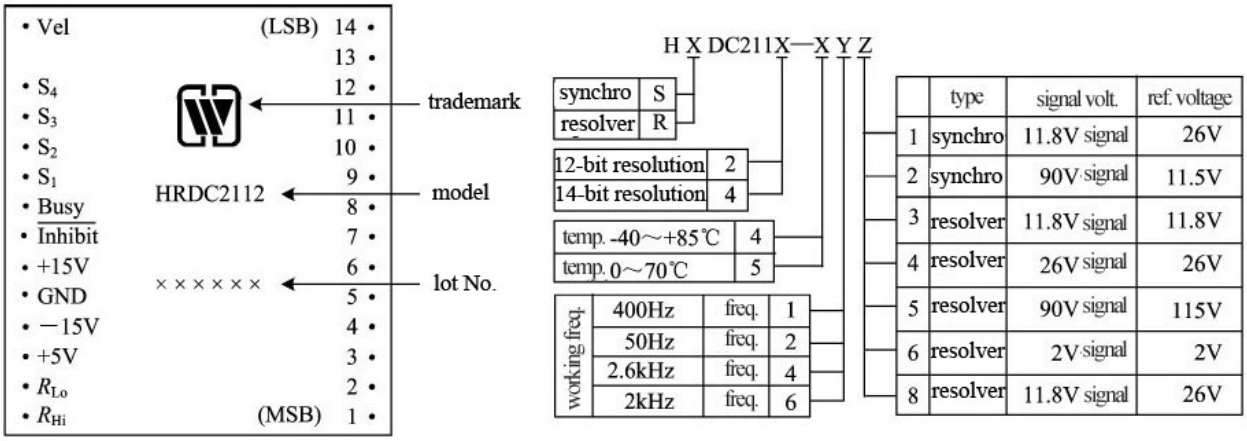
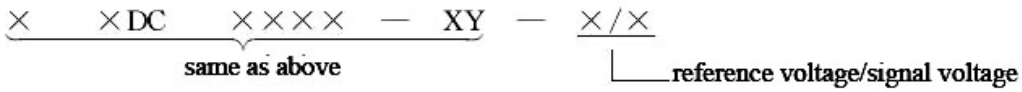


Fig.11 Part numbering key

Note: when the above signal voltage and reference voltage (Z) are non-standard, they shall be given as follows:



(e.g. reference voltage 5V and signal voltage 3V are expressed as -5/3)

Application notes:

- ✧ Supply the power correctly, upon power-on, be sure to correctly connect the positive and negative pole of the power supply for fear of burning.
- ✧ Upon assembly, the bottom of the product shall fit to the circuit board closely so as to avoid damage of pins, and shockproof provision shall be added, if necessary.
- ✧ When the user places an order for the product, detailed electric performance indexes shall refer to the relevant enterprise standard.