Synchro/Resolver-Digital Converter
(MSDC/MRDC37 series)

1. Features (for outside view, see Fig. 1)

- High accuracy
- Small size
- High tracking speed
- Uninterrupted tracking during data transfer
- Three-state latch output
- Low power consumption

Size: 50.8x50.8x10mm^3; weight: 48g

Fig.1 Outside view of MSDC/MDRC37 series

2. Application

Servo mechanism; antenna monitoring; navigation system; cannon control; industrial control; robot system; radar control system.

3. Description

MSDC/MRDC37 series are 16-bit digital-to-synchro/resolver converters. The input signal is divided into four-wire resolver and excitation signal or three-wire synchro and excitation signal. The output signal is parallel natural binary code buffered through three-state latch and compatible with TTL level.

The product applies second-order servo circuit with small size and light weight, and the user can use it very conveniently by controlling signal pins.

Table 2 Rated conditions and recommended operating conditions

Max. absolute rating value	Supply voltage $+V_S$: 12.5~17.5V Supply voltage $-V_S$: -17.5~-12.5V Logical voltage V_L: 7V Storage temperature range: -40~+100℃
Recommended operating conditions	Supply voltage $+V_S$: 15V±5% Supply voltage $-V_S$: -15V±5% Reference voltage (effective value) V_{Ref}: nominal value ±10% Signal voltage (effective value) V_1*: nominal value ±10% Reference frequency f*: nominal value ±10% Operating temperature range T_A: -40~+85℃

Table 2 Electric characteristics

Parameter	Conditions (-40~+85℃) (Unless otherwise specified)	(MSDC/MRDC37 series) Min.	Max.	Unit
Resolution/RES	Range of 0~360º	12	16	Bit
Tracking speed/S_t ①	–	3	36	rps
High output level/V_{OH}	T_A=25℃	2.4	–	V
Low output level/V_{OL}	T_A=25℃	–	0.8	V
Power consumption/ P_D	T_A=25℃	–	1.3	W
Vel linearity/E_{Rl}	T_A=25℃	–	1.0	%
Range of reference voltage	–	2	115	V
Range of signal voltage	–	2	90	V
Frequency range	–	30	2 600	Hz
Density	–	±3	±8.5	Angular minute

Note: ① the tracking speed is 3 rps for 16-bit resolution and 36 rps for 12-bit resolution; S_t can be designed according to the user's requirement.

5. Operating principle (Fig. 2)

The synchro input signal (or input signal of resolver) is converted into the orthogonal signal through internal differential isolation:

$$V_1 = KE_0 \sin\theta \sin\omega t \ , V_2 = KE_0 \cos\theta \sin\omega t$$

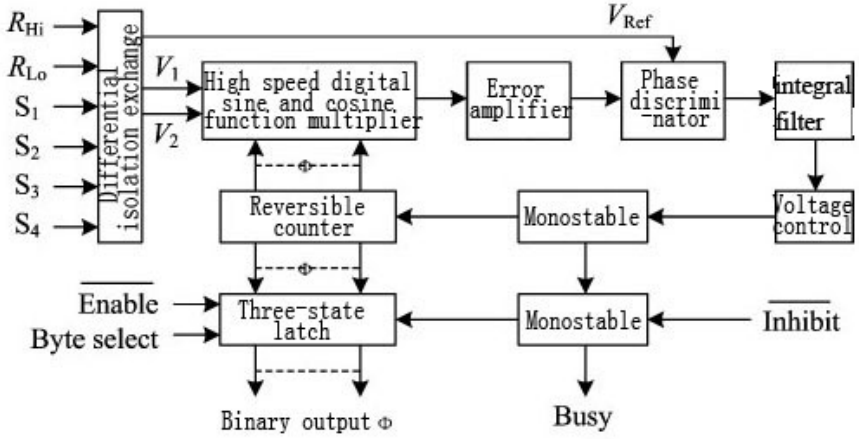

Fig.2 Block diagram for operating principle

Where, θ is analog input angle

These two signals and the digital angle φ of internal reversible counter are multiplied in the multiplier of Sine and Cosine functions and are error treated:

$$KE_0 \sin\theta\cos\varphi\sin\omega t - KE_0\cos\theta\sin\varphi\sin\omega t = KE_0 \sin(\theta-\varphi) \sin\omega t$$

The signals are sent to voltage controlled oscillator after amplification, phase discrimination and integration filtration, if θ-φ≠0 , the voltage controlled oscillator will output pulse to change the data in the reversible counter, till θ-φ becomes zero within the accuracy of the converter, during this process, the converter tracks the change of input angle θ all the time. For the block diagram of working principle, see Fig. 2.

Transfer function of the converter is shown in Fig. 3.

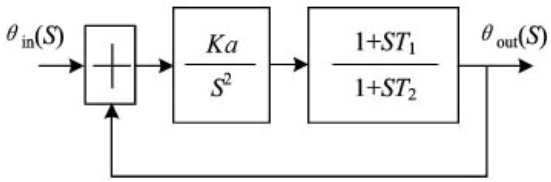

Fig. 3 Function transfer of the converter

Closed-loop function

$$\frac{\theta_{in}(S)}{\theta_{out}(S)} = \frac{1+T_1S}{1+ST_1+S^2/Ka+S^3T_2/Ka}$$

Methods of data transfer and time sequence

There are two methods for reading the effective data in the converter: synchronous reading and asynchronous reading.

(1) $\overline{\text{Inhibit}}$ method (synchronous reading):

A: the converter is connected with 16-bit bus. Bysel is connected with logic “1”.

Set $\overline{\text{Inhibit}}$ from logic “1” to logic “0” (data lock), and wait for 1μs; set $\overline{\text{Enable}}$ to logic “0” to allow the latch in the converter to output data; read 12-bit, 14-bit or 16-bit data; set $\overline{\text{Inhibit}}$ to logic “1” in order to get ready for reading the next effective data (Fig. 4);

B: the converter is connected to 8-bit bus, D_1~D_8 bit are connected to data bus, and the rest are empty.

Set $\overline{\text{Inhibit}}$ from logic “1” to logic “0” (data lock), and wait for 1μs; set $\overline{\text{Enable}}$ to logic “0” to allow the latch in the converter to output data; set Bysel to logic “1”, directly read the high 8-bit data, set Bysel to logic “0”, read the data in other bits with automatic zero padding in the vacant bits; set $\overline{\text{Inhibit}}$ to logic “1” in order to get ready for reading the next effective data (Fig. 5).

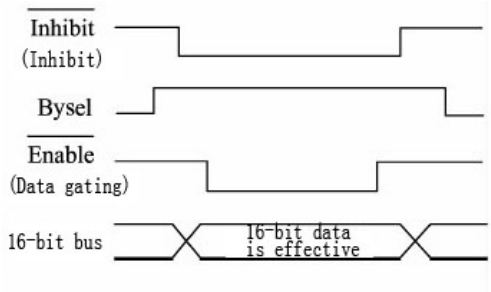

Fig4 Time sequence of 16-bit bus transfer

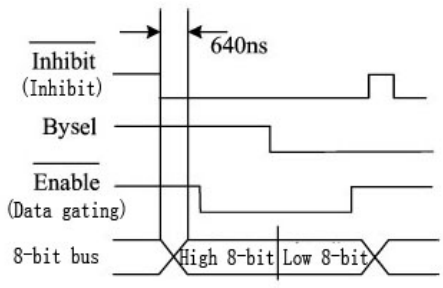

Fig5 Time sequence of 8-bit bus transfer

(2) Busy method (asynchronous reading):

In asynchronous reading mode, $\overline{\text{Inhibit}}$ is set to logic "1" or empty, whether the internal loop is always in the stable state or whether the output data is valid shall be determined through the status of busy signal **Busy**. When Busy signal is at high level, it indicates the data is being converted, and the data at this time is unstable and invalid; when Busy signal is at low level, it indicates the data conversion has been completed, and the data at this time is stable and valid. Once high level occurs in Busy during reading, the reading at this time is invalid. In asynchronous reading mode, the Busy output is pulse train of TTL level, its width depends on its rotational speed, there are also two use methods of the bus, i.e. 8-bit and 16-bit, the data reading during effective data output is also controlled by $\overline{\text{Enable}}$, please refer to the time sequence diagram for data transfer (Fig. 6 and Fig. 7).

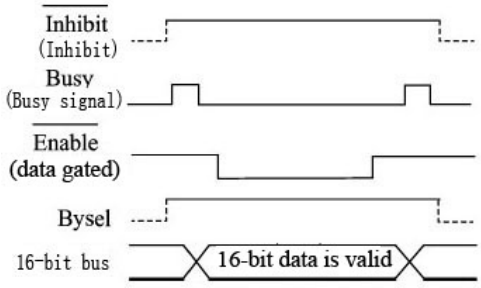

Fig.6 Time sequence diagram for 16-bit bus transfer

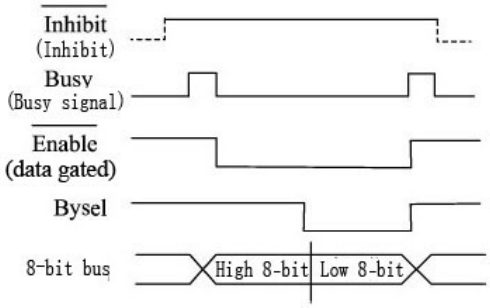

Fig.7 Time sequence diagram for 8-bit bus transfer

Status signal pins: Busy, DIR, R, C.

When the input of the converter changes, Busy outputs a train of pulses of CMOS level, its frequency is determined by the highest rotational speed. When Busy is at high level, it means the second-order servo circuit in the converter is operating, the data at digital output end is changing; on the contrary, the computer can directly read the data.

DIR signal is used to indicate forward/reverse rotation. When the output code is up count, the output is high level; when the output code is down count, the output is low level.

Zero signal output R.C: when the output data increments from all "1" to all "0", or the output data decrements from all "0" to all "1", the output is positive pulse, the pulse width is 200μs.

6. MTBF curve (Fig. 7)

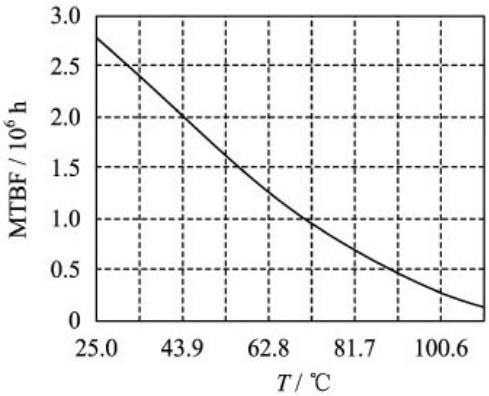

Fig. 8 MTBF-temperature curve

(Note: as per GJB/Z299B-98, envisaged good ground condition)

7. Pin designation (Fig. 9, Table 3)

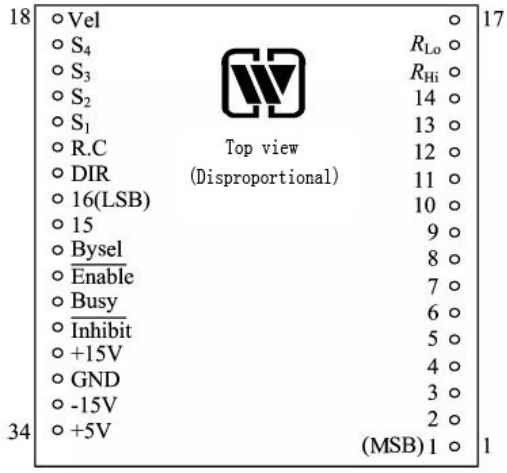

Fig.9 Pin designation (top view)

Table 3 Pin designation

Pin	Symbol	Meaning	Pin	Symbol	Meaning	Pin	Symbol	Meaning
1	D_1	Digital output 1 (highest bit)	13	D_{13}	Digital output 13	25	D_{16}	Digital output 16
2	D_2	Digital output 2	14	D_{14}	Digital output 14	26	D_{15}	Digital output 15
3	D_3	Digital output 3	15	R_{Hi}	Reference signal input (high end)	27	Bysel	Byte select signal
4	D_4	Digital output 4	16	R_{Lo}	Reference signal input (low end)	28	$\overline{\text{Enable}}$	Enable signal
5	D_5	Digital output 5	17	NC	Dead end	29	Busy	Busy signal
6	D_6	Digital output 6	18	Vel	Velocity voltage output	30	$\overline{\text{Inhibit}}$	Inhibit signal
7	D_7	Digital output 7	19	S_4	Signal input	31	+Vs	+15V Power supply
8	D_8	Digital output 8	20	S_3	Signal input	32	GND	Power ground
9	D_9	Digital output 9	21	S_2	Signal input	33	-Vs	-15V Power supply
10	D_{10}	Digital output 10	22	S_1	Signal input	34	V_L	+5V Power supply
11	D_{11}	Digital output 11	23	R, C	Zero cross signal			
12	D_{12}	Digital output 12	24	DIR	Direction signal			

Notes: S_1, S_2, S_3, S_4 are signal input of synchro/resolver, and S_4 is left unconnected for synchro;
D_1~D_{16} are binary data output, for MSDC/MRDC3752 series converter, pin 13, 14, 25 and 26 are left unconnected;
for MSDC/MRDC3754 series converter, pin 25 and 26 are left unconnected.

8. Table of weight values (Table 4)

Table 4 Table of weight values

Bit	Angle	Bit	Angle	Bit	Angle
1(MSB)	180,000 0	7	2,812 5	13	0,043 9
2	90,000 0	8	1,406 3	14	0,022 0
3	45,000 0	9	0,703 1	15	0,011 0
4	22,500 0	10	0,351 6	16	0,005 5
5	11,250 0	11	0,175 8		
6	5,625 0	12	0,087 9		

9. Connection diagram for typical application (Fig. 10 and Fig. 11)

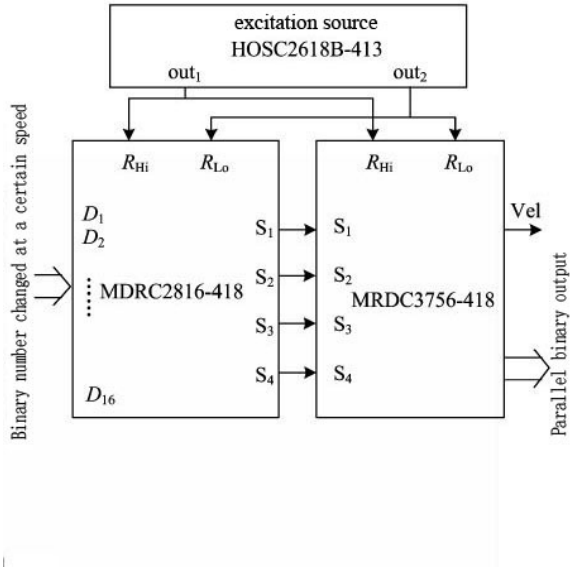

Fig.10 Connection diagram for typical application of MRDC3756 series

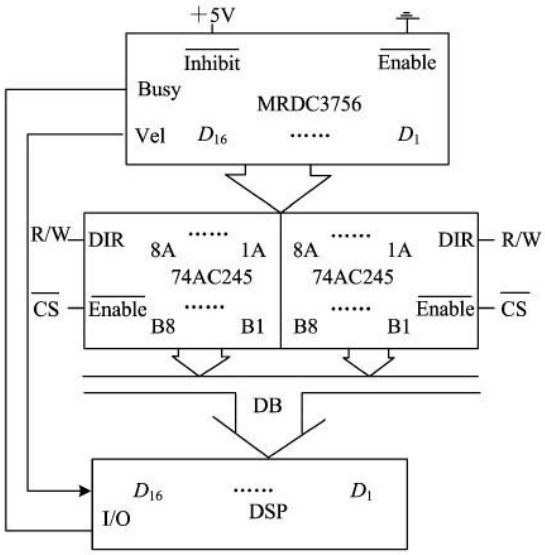

Fig.11 Interface for direct data reading of MRDC3756

Note: the supply voltage shall not exceed the specified range; do not connect reference R_{Hi} and R_{Lo} to other pins.

10. Package specifications (unit: mm) (Fig. 12)

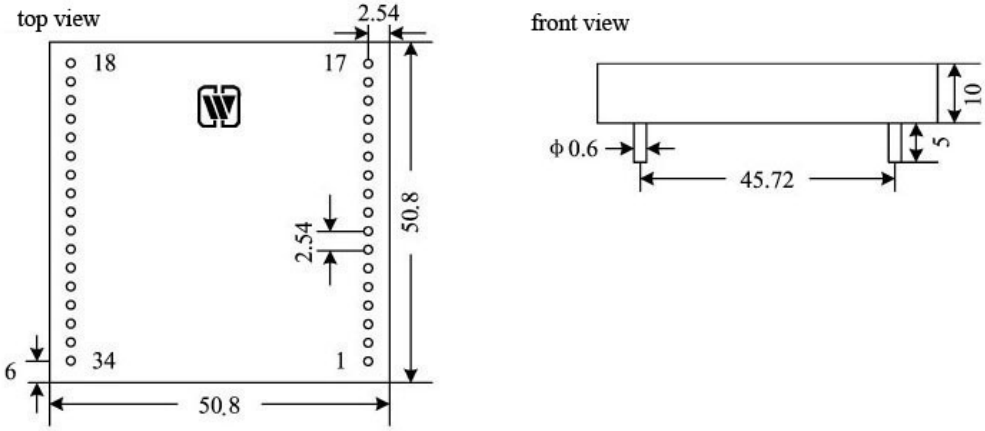

Fig. 12 Outside view and dimensions of package

11. Part numbering key (Fig. 13)

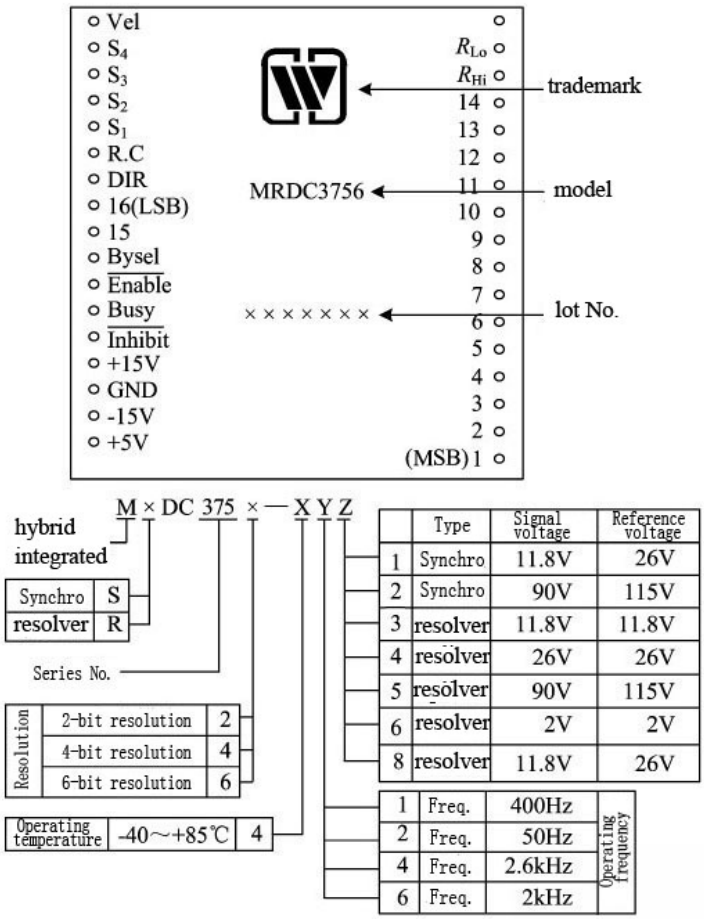

Fig. 13 Part numbering key

Note: when the above signal voltage and reference voltage (Z) are non-standard, they shall be given as follows:

M ×DC 375× — XY — ×/×

Ditto | Reference voltage/signal voltage

(e.g. reference voltage 5V and signal voltage 3V are expressed as -5/3)

Application notes:

- ✧ Supply the power correctly, during the power-up, accurately connect the positive and negative poles of power to avoid burnout.
- ✧ When the max. absolute rating value is exceeded, the device may be damaged.
- ✧ Upon assembly, the bottom of the product shall fit to the circuit board closely so as to avoid damage of pins, and shockproof provision shall be added, if necessary.
- ✧ When the user places an order for the product, detailed electric performance indexes shall refer to the relevant enterprise standard.