Synchro/Resolver-to-Digital Converter (Series HSDC/HRDC174)

1 FEATURES (Outline is shown in Fig 1, Classifications are shown in Tab 1.)

- Internal differential isolation transfer
- Resolution:12bit, 14bit
- 3-state output latches
- Continuous high tracking rate
- 32-pin salt fog resistant metal case package
- MCM high-density package
- ESD 2000V
- Pin-to-pin compatible with AD Company SDC/RDC1740/1741/1742 product

Size: 44.2×28.9×7.2mm^3

Weight:22g

Figure 1 Series HSDC/HRDC174 outline

2 APPLICATIONS

- Flight instrument systems
- Artillery control systems
- Avionic control systems
- Radar control systems
- Ship navigation systems
- Antenna monitoring systems
- Robotics system
- CNC machine

Other automatic control systems

Table 1 Product classification

12 bit		14 bit	
synchro	resolver	synchro	resolver
HSDC1742－X11	HRDC1742－X13	HSDC1744－X11	HRDC1744－X13
HSDC1742－X12	HRDC1742－X14	HSDC1744－X12	HRDC1744－X14
HSDC1742－X41	HRDC1742－X18	HSDC1744－X41	HRDC1744－X18
HSDC1742－X42	HRDC1742－X23	HSDC1744－X42	HRDC1744－X23
HSDC1742－X21	HRDC1742－X24	HSDC1744－X21	HRDC1744－X24
HSDC1742－X22	HRDC1742－X28	HSDC1744－X22	HRDC1744－X28
	HRDC1742－X43		HRDC1744－X43
	HRDC1742－X44		HRDC1744－X44
	HRDC1742－X48		HRDC1744－X48

3 GENERAL DESCRI PTION

Series HSDC/HRDC174 are 12 or 14 bit hybrid integrated continuous tracking synchro/resolver-to-digital converters. The series are fabricated using MCM process. Core devices are specific chips developed by our Institute. They are packaged by 32-pin DIP shallow-cavity salt fog resistant metal cases. They feature small sizes and light weights and are pin-to-pin compatible with AD Company SDC/RDC1740/1741/1742 product.

The design and manufacture of Series HSDC/HRDC174 meet demands of GJB2438A-2002 《Hybrid integrated circuit general specifications》 and products detailed specifications. Quality assurance grade is H.

4 TECHNICAL SPECIFICATIONS (Tab 2, Tab 3)

Table 2 Nominal conditions and recommended working conditions

Absolute max nominal value	power supply voltage Vs:±17.25V_{DC} Logical power supply voltage V_L:+7V_{DC} Storage temperature range:-65~+150℃
Recommended working conditions	power supply voltage Vs:±15±0.75V 5V power supply voltage 5±0.25V reference voltage effective value Vref*:115V,26V,11.8V signal voltage effective value V_I*: 90V, 26V,11.8V reference frequency f: 400Hz,50Hz,2.6kHz operating temperature range T_A: -55~+125℃

* means that it can be made to order.

Table3 Electrical characteristics(-55~+125℃)

Characteristics			SeriesHSDC /HRDC1742	SeriesHSDC /HRDC1744	Units	Comments
Accuracy			±8.5(max)	±5.3(max)	Arc min	
Tracking rate			36(typ)	27(typ)	Rev/s	
Resolution			12	14	bit	
Signal/Reference frequency			50~2600	50~2600	Hz	
Signal input voltage			2~90	2~90	V	
Reference input voltage			2~115	2~115	V	
Signal input impedance	90V signal	single-end differential	100 200	100 200	kΩ kΩ	
	26V signal	single-end differential	28 56	28 56	kΩ kΩ	
	11.8Vsignal	single-end differential	13 26	13 26	kΩ kΩ	
Reference input impedance	115V ref	single-end differential	127 254	127 254	kΩ kΩ	
	26V ref	single-end differential	28 56	28 56	kΩ kΩ	
	90V ref	single-end differential	100 200	100 200	kΩ kΩ	
Acceleration constant			80000(min)	56000(min)	Sec^{-2}	Design guaranteed
Step response			75(max)	100(max)	ms	
Power supply current	+ Vs=+15V		35(max)	35(max)	mA	
	- Vs=+15V		35(max)	35(max)	mA	
	$V_{L=}$+5V		56(max)	56(max)	mA	
Power dissipation			1.4(max)	1.4(max)	W	
Enable Inhibit Busy pulse width Load capacity	establishment or release time establishment time		80(max) 640(max) 200~600(typ400) 2(min)	80(max) 640(max) 200~600(typ400) 2(min)	ns ns ns TTL	
Digital output	V_{OH}		3.3(min)	3.3(min)	V_{DC}	
	V_{OL}		0.7(max)	0.7(max)	V_{DC}	
	Load capacity		3(max)	3(max)	TTL	
Operating temperature range Select 8YZ			-55~+125	-55~+125	℃	

5 CIRCUIT THEORY DIAGRAM (Fig 2, Fig 3)

Internal differential isolation converts input signals of synchro(resolver) into orthogonal signals:

$Vsin=KE_0 sin(\omega t+\alpha)sin\theta$ (sin)

$Vcos=KE_0 sin(\omega t+\alpha)cos\theta$ (cos)

Where θis analogue input angle.

The two signals are multiplied by digital angle φ of internal reversible counter in sin/cos multiplier, thus result in error signal:

$KE_0 sin(\omega t+\alpha)(sin\theta cos\varphi - cos\theta sin\varphi)$

i.e. $KE_0 sin(\omega t+\alpha)\ sin(\theta-\varphi)$

After magnification, phase demodulator and integrator, the signal is inputted into VCO. If $\theta-\varphi\neq 0$, VCO will output pulse, up/down counter will count until $\theta-\varphi=0$. During this process, converter continuously tracks changes of input angle.

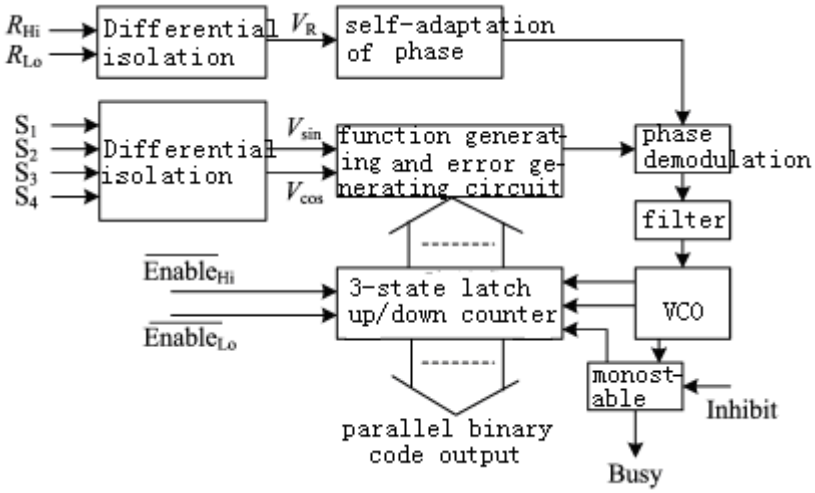

Figure2 Functional block diagram

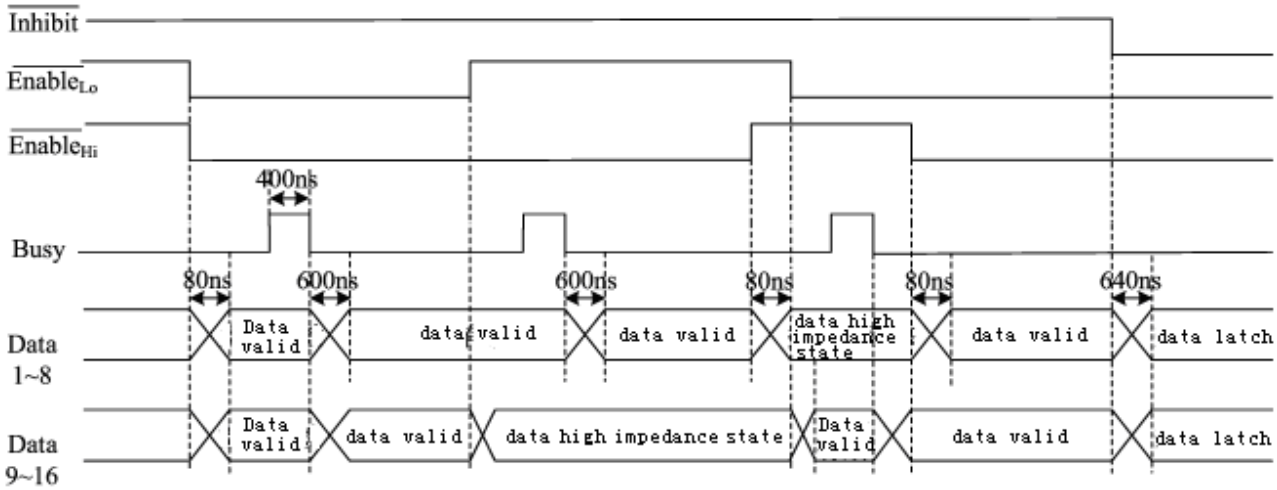

Figure3 Timing diagrams during bus transmission

$\overline{Inhibit}$

$\overline{Inhibit}$ logic input only inhibits data transfer from up/down counter to output latch. It does not interrupt work in tracking circuit. When releasing Inhibit, the system will automatically generate a pulse to update output data.

$\overline{\text{Enable}}$

$\overline{Enable_{Lo}}$, $\overline{Enable_{Hi}}$ inputs determined the state of output data. When set to a logic high, output pin is in the high impedance state. When set to a logic low, data in latch are transferred to output pin. $\overline{Enable_{Hi}}$ enables high 8 bit data, while $\overline{Enable_{Lo}}$ enables low 6 bit data(HSDC/HRDC1742 are. low 4 bit data).

Busy

When input of the converter changes, Busy outputs a series of CMOS level pulses. Their frequencies are determined by maximal rotating speed. Falling edge of Busy pulse triggers latch to update data. After 600s of maximum delay, output data are valid. Typical width of Busy pulse is 400ns, output load capacity is 3TTL.

(1) data transfer method and timing

Two methods that follow can be used in data transfer:

① $\overline{Inhibit}$ method

After 640ns of $\overline{Inhibit}$ logic low, output data are valid. Data transfer is realized through $\overline{Enable_{Lo}}$ and $\overline{Enable_{Hi}}$. After releasing Inhibit, the system automatically generates a pulse which is equivalent to Busy pulse width and is used in data update.

② Busy method

At rising edge of Busy pulse, 3-state up/down counter counts. At falling edge of Busy pulse, Latch pulse that has the same width as Busy pulse is generated inside and is used to update data from 3-state latch. Data transfer timing is shown in fig 3, i.e. after 600ns of Busy logic low, data are stable and transmission is valid. When asynchronous reading method is used, Busy outputs CMOS level pulse series, which width of high, low level is relevant to operating frequency and rotating speed of the selected device.

(2) Compatibility

When used under non-nominal signal and non-nominal reference voltage conditions, signal and exciting input pins of series HSDC/HRDC174 are serially connected to ratio resists, realizing compatibility.

Example1: HSDC1742-411 is used in connection with 36V/26V/400Hz(exciting voltage/signal voltage/frequency), shown in fig.4

Example2: HRDC1742-418 is used in connection with 36V/26V/400Hz(exciting voltage/signal voltage/frequency), shown in fig.5

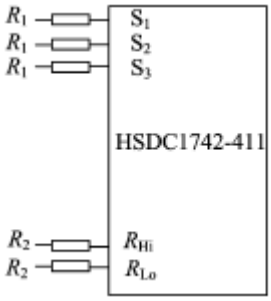

Figure4 HSDC1742-411 connection

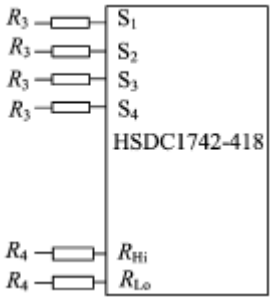

Figure5 HSDC1742-418 connection

R1=(V_I- V_I nominal value)×1.11k=(26V-11.8V)×1.11k=15.8kΩ
R2=(V_{Ref}- V_{Ref} nominal value)×1.11k=(36V-26V)×1.11k=11.1kΩ
R3=(V_I- V_I nominal value)×1.11k=(26V-11.8V)×1.11k=15.8kΩ
R4=(V_{Ref}- V_{Ref} nominal value)×1.11k=(36V-26V)×1.11k=11.1kΩ

(3) Dynamic performance

The transfer function of the converter is given in fig.6.

Open loop gain:

$$\frac{qout}{qin}=\frac{Ka}{S^2}*\frac{1+ST_1}{1+ST_2}$$

Closed loop gain:

$$\frac{qout}{qin}=\frac{Ka}{S^2}*\frac{1+ST_1}{1+ST_1+\frac{S^2}{Ka}+\frac{S^3T_2}{Ka}}$$

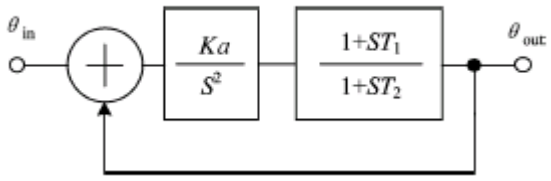

Figure6 Transfer function

Model HSDC/HRDC 1742
Where Ka=80000, T_1=0.0087, T_2=0.001569

(4) Acceleration error

A tracking converter employing a type Ⅱ servo loop does not suffer any velocity lag, however, there is additional error duo to acceleration. This additional error can be defined using the acceleration constant Ka of the converter.

$$Ka=\frac{Input\ \ acceleration}{Error\ \ in\ \ outpu\,t\ \ an\,gel}$$

for example, Ka can be used to calculate tracking error of 14 bit converter HSDC1744:
Ka=56000, acceleration=50 revolutions/sec^2,

$$\text{Error in least significant bits(LSBs)}=\frac{50\times 16384}{56000}=14.62LSBs$$

6 TYPICAL PERFORMANCE CURVES (Fig7, Fig 8)

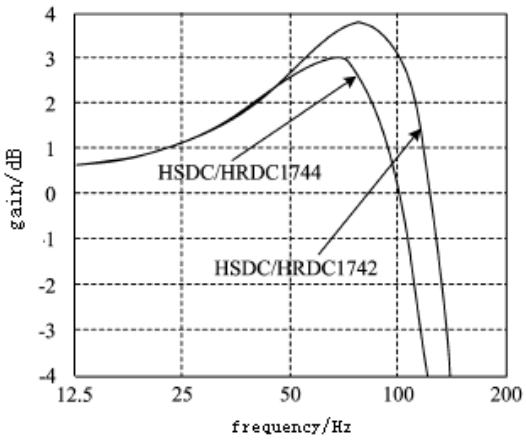

Figure7 HSDC/HRDC1742 gain plot

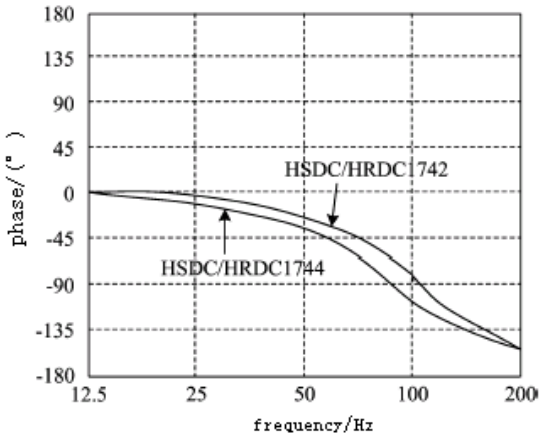

Figure8 HSDC/HRDC1742 phase plot

7 MTBF DIAGRAM (Fig 9)

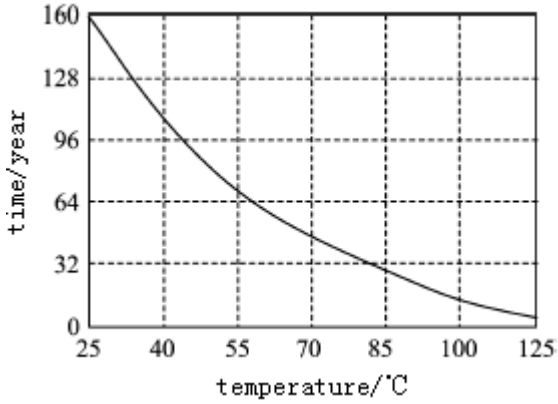

Figure 9 MTBF vs. temperature

(Note: According to GJB/Z 299B-98, assuming that ground is in good condition)

8 PIN CONFIGURATIONS (Fig 10, Tab4)

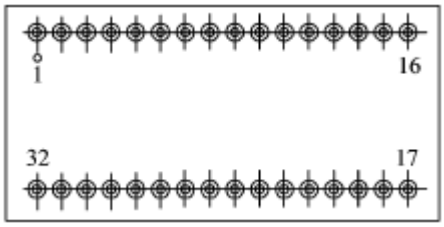

Figure 10 Pin out (bottom view)

Table 4 Pin description

Pin	mnemonic	description	Pin	mnemonic	description
1	D1	Digit output 1(MSB)	17②	NC/S4	Not connected/resolver input S4
2	D2	Digit output 2	18	S3	Resolver/synchro input S3
3	D3	Digit output 3	19	S2	Resolver/synchro input S2
4	D4	Digit output 4	20	S1	Resolver/synchro input S1
5	D5	Digit output 5	21	NC	Not connected
6	D6	Digit output 6	22	NC	Not connected
7	D7	Digit output 7	23	Case	Case
8	D8	Digit output 8	24④	NC(or Vel)	Not connected(or velocity output pin)
9	D9	Digit output 9	25	$\overline{Enable}_{Lo}$	Enable low 4bit/6bit
10	D10	Digit output 10	26	$Enable_{Hi}$	Enable high 8bit
11	D11	Digit output 11	27	$\overline{Busy}$	“Busy” signal
12	D12	Digit output 12	28	$\overline{Inhibit}$	inhibit pin
13③	NC/D13	Not connected/ Digit output13	29	+Vs	+15V power supply
14③	NC/D14	Not connected/ Digit output14	30	GND	ground
15	R_{Lo}	Input pin for reference low	31	- Vs	-15V power supply
16	R_{Hi}	Input pin for reference high	32	V_{Lo}	+5V power supply

Note: ①for series HSDC1742, HRDC1742 converters, pin 13 and 14 are not connected.

②for HSDC174X, pin 17 is not connected, for HRDC174X, pin 17 is resolver input S4

③ for series HSDC1742, HRDC1742 converters, pin 25 is enable low 4 bit control

④when there is need for velocity, connect pin 24

9 BIT WEIGHT TABLE (Tab 5)

Table 5 Bit weight table

Bit number	Weight (degrees)	Bit number	Weight (degrees)	Bit number	Weight (degrees)
1(MSB)	180.0000	6	5.6250	11	0.1758
2	90.0000	7	2.8125	12(12 bit LSB)	0.0879
3	45.0000	8	1.4063	13	0.0439
4	22.5000	9	0.7031	14(14 bit LSB)	0.0220
5	11.2500	10	0.3516		

10 CONNECTION OF TYPICAL APPLICATION (Fig 11)

Description:

(1) Voltages on pin 29,31 should be ±15V, should not be reversed, connect digital logic power supply +5V to pin32.

(2) 0.1μF ceramic and 6.8μF electrolytic capacitor should be parallelly connected between power supply and ground.

(3) Pin marked case is connected to case

(4) For HSDC/HRDC 1742, digital outputs are from pin1 to pin12, pin13,14 are not connected.

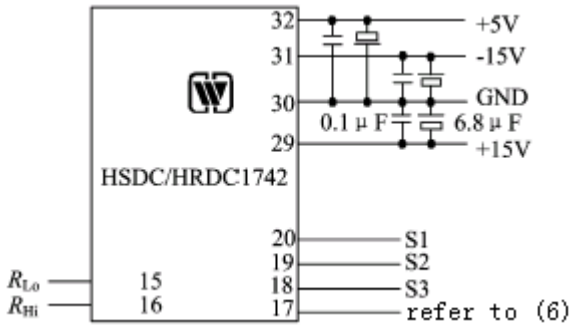

Figure 11 Connection of typical application

(5) Reference connections are connected to Pin15R_{lo} and 16R_{hi}.

In the case of synchro, by convention, signals are connected to S_1,S_2,S_3.

$$E_{S_1\sim S_3} = E_{R_{Lo}\sim R_{Hi}} \sin(\omega t + a)\sin\theta$$
$$E_{S_3\sim S_2} = E_{R_{Lo}\sim R_{Hi}} \sin(\omega t + a)\sin(\theta + 120^\circ)$$
$$E_{S_2\sim S_1} = E_{R_{Lo}\sim R_{Hi}} \sin(\omega t + a)\sin(\theta + 240^\circ)$$

In the case of resolver, by convention, signals are connected to S_1,S_2,S_3,S_4.

$$E_{S_1\sim S_3} = E_{R_{Lo}\sim R_{Hi}} \sin(\omega t + a)\sin\theta$$
$$E_{S_2\sim S_4} = E_{R_{Lo}\sim R_{Hi}} \sin(\omega t + a)\cos\theta$$

(6) For resolver, pin 17 is S_4, for synchro, pin 17 is not connected.

11 PACKAGE OUTLINE DIMENTION AND DISCRIPTION

(Unit: mm**) (** Fig. 12, Tab 6&7 **)**

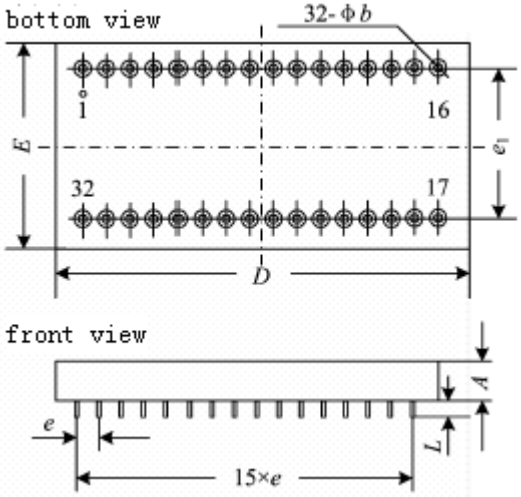

Figure 12 Package outline drawing

Table 6 Symbol nominal

symbol	nominal value
A	7.2
ϕb	0.45
D	44.2
E	28.9
e	2.54
e_1	22.86
L	5min

Table 7 Packaging case descriptions

Case model	Base material	Base coat	Lid(cap) material	Lid(cap) coat	Lead material	Lead coat	Sealing method	comments
UP4429-32a	Kovar (4J29)	Ni	Fe/Ni alloy	Ni	Kovar (4J29)	Ni/Au	Match sealing	Pin 23 coat is Ni

Note: The temperature of soldered pins does not surpass 300℃ within 10 sec.

12 DESCRIPTIONS OF PRODUCT MODEL NUMBERING (Fig. 13)

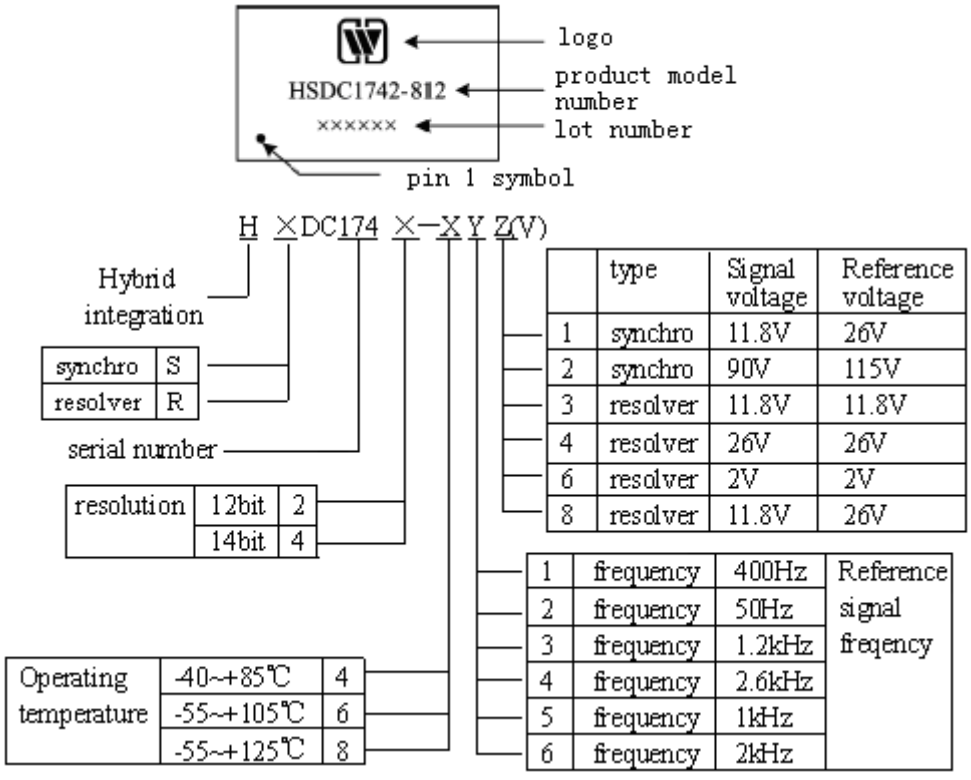

Table 13 Descriptions of product name

Note: When signal voltage and reference voltage(Z) above are not nominal, product name is given as follows:

(for example, reference voltage is 5V, signal voltage is 3V, name denotes 5/3)

Application Notes:

★Polar voltage of power supply should be correct.

★When exceeding absolute maximum nominal value, it will possibly lead to damage to the device.

★While assembling, the bottom of the product should be placed close to the board to avoid damage to the pins. If necessary, take shockproof measures.

★Leads avoid bending, or it will easily lead to crack of insulator, which affects hermeticity.

★When product is ordered, detailed electrical performance specifications should be referred to corresponding business standard.