Programmable 2-speed SDC/RDC Converter (Series HTS20)

1 FEATURES (Outline is shown in Fig 1, Classifications are shown in Tab 1.)

- Complete 2-speed system
- Programmable speed ratios in coarse/fine channel
- 1:8, 1:16, 1:32, 1:64
- Digital output with 3-state latches
- Maximum resolution is 20 bit
- Maximum accuracy is 5 Arcsec

Size: 59.3×59.3×7.8mm^3

Weight: 70g

Figure 1 Series HTS20 outline

Table 1 Product classification

HTS20R-418
HTS20R-668
HTS20R-618
HTS20R-658

2 APPLICATIONS

- Radar monitoring
- Tracking navigation
- Satellite tracking
- Artificial technology
- Artillery control
- Industrial machine control

Other high-accuracy measurement

3 GENERAL DESCRI PTION

Series HTS20 programmable 2-speed SDC/RDC converter are single module hybrid integrated circuit packaged in metal case. They internally contain coarse/fine two way synchro/resolver-to-digital converter and error correcting logical circuit required by two way system.

Speed ratios of coarse/fine combination of Series HTS20 products are 1:8, 1:16, 1:32, 1:64，the required speed ratio can be obtained by external program. It is convenient to use. Two way coarse/fine input signals are signals of three-wire synchro or four-wire resolver.

Series HTS20 programmable 2-speed SDC/RDC converter output natural parallel binary codes. Maximum is up to 20bit. They have 3-state latches.

4 TECHNICAL SPECIFICATIONS

(Tab 2, Tab 3)

Table 2 Nominal conditions and recommended operating conditions

Absolute max nominal value	Power supply voltage Vs:±17V Logical power supply voltage V_L:+7V Storage temperature range:-55~+105℃
Recommended working conditions	Power supply voltage Vs:±15V Power supply voltage V_L: +5V Reference voltage effective value V_{Ref}*: 2~115V Signal voltage effective value V_I*: 2~90V Reference frequency f*: 50Hz~10kHz Operating temperature range T_A: -40~+85℃ -55~+105℃

* means that it can be made to order.

Table3 Electrical characteristics

Characteristics	Conditions	HTS20R/HTS20S Business military standard (Q/HW30925-2006)		Units	Comments
		Min	Max		
Resolution (optionally controlled by SC1, SC2)	speed ratio 1:8 1:16 1:32 1:64	 - - - -	 17 18 19 20	bit	
Accuracy(0 ° ~360 °)	speed ratio 1:8 1:16 1:32 1:64	 - - - -	 40 20 10 5	Arc sec	
Fine channel tracking velocity	400Hz	-	36	Rev/s	
Frequency range	-	50	10k	Hz	
Exciting voltage range(effective value)	-	2	115	V	
Signal voltage range(effective value)	-	2	90	V	

5 CIRCUIT THEORY DIAGRAM (Fig 2, Fig 3)

(1) Single speed converter

The principles of operation of single speed converter are shown in fig2., principles are summarized as follows:

Internal differential isolation converts input signals of synchro(resolver) into orthogonal signals:

$V_1=KE_0\sin\theta\sin\omega t$, $V_2=KE_0\cos\theta\sin\omega t$

Where θis analogue input angle.

The two signals are multiplied by digital angle φ of internal up/down counter in sin/cos multiplier, thus result in error signal:

$KE_0\sin\theta\cos\varphi\sin\omega t - KE_0\cos\theta\sin\varphi\sin\omega t = KE_0\sin(\theta-\varphi)\sin\omega t$

After error magnification, phase demodulator and integrator, the signal is inputted into VCO. If $\theta-\varphi\neq 0$, VCO will output pulse, up/down counter will count until$\theta-\varphi=0$. During this process, converter continuously tracks changes of input angle.

(2) 2-speed converter

The principles of operation of 2-speed converter are shown in fig3. The operation of the coarse and fine channel of the 2-speed converter is the same as above-mentioned single speed, but 2-speed converter consists of two sets of single speed converter and programmer error logical circuit. Coarse channel fulfills conversion from 10~12bit logical angle to digital angle. Fine channel fulfills conversion from 14bit logical angle to digital angle. digital angles converted by Coarse channel and Fine channel are inputted into programmer error-correcting logical circuit respectively. After error processing and correcting, it will output a 20bit parallel binary digit, which is inputted into output latch and buffered to output digital angle, fulfilling the entire conversion.

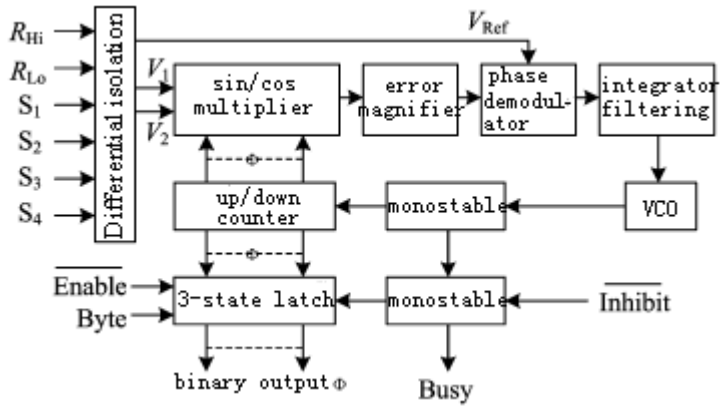


Figure2 Functional block diagram of single speed converter

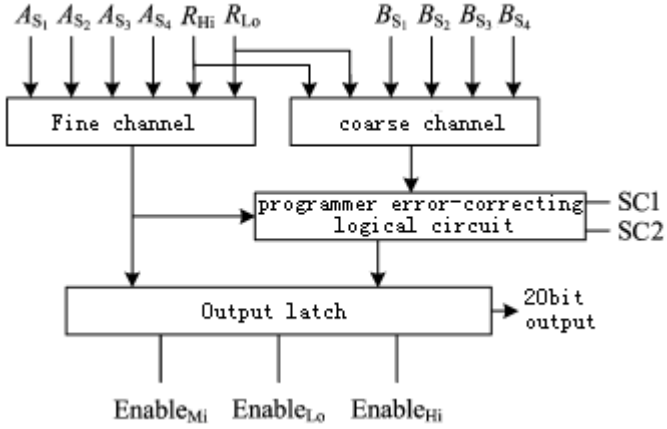


Figure3 Functional block diagram of 2-speed converter

(3) Data transfer method and timing

Outputs of series HTS20 2-speed converters reach 20bit. Through $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ which take 3-state control of output latch, 2-speed converter can be easily connected to data bus. $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ are all valid at low level. $Enable_{Lo}$ controls low 8bits, $Enable_{Mi}$ controls middle 8bits, $Enable_{Hi}$ controls rest high bits.

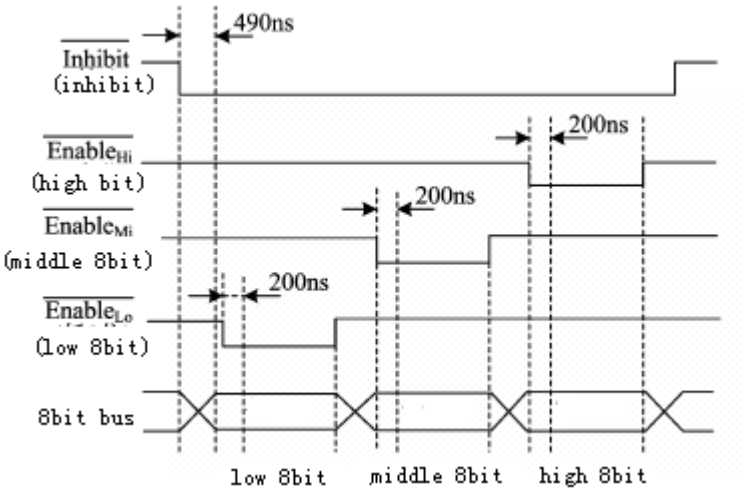


Figure 4 Timing diagrams during 8bit bus transmission

Data of series HTS20 2-speed converters are read as follows:

Set $\overline{Inhibit}$ to logical "0", after 490μm, data in 3-state latch of the converter are upgraded. It can read data of low 8bits, middle 8bits and high bits through controlling $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$.

Figure 4 Gives timing of reading data when 2-speed converter and 8 bit data bus are connected.

To ensure high-accuracy conversion of 2-speed converter, please pay attention to the following:

① Amplitudes of input signals of coarse and fine channels should be guaranteed within nominal value 10%.

② Frequencies of input signals and reference signals of coarse and fine channels should be the specified operating frequencies.

③ Phase shift between input signal and reference signal of coarse channel and phase between input signal and reference signal of fine channel should be less than 10°.

④ Wave distortions of input signals and reference signals of coarse and fine channels should be less than 5%.

⑤ Variation of +5V, ±15V power supply should be guaranteed within ±5%.

6 MTBF DIAGRAM (Fig 5)

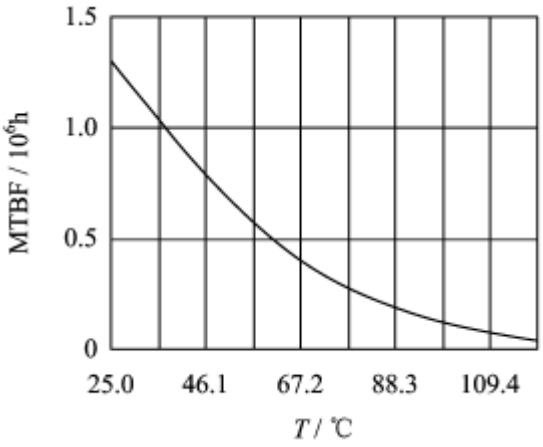


Figure 5 MTBF vs. temperature

(Note: According to GJB/Z 299B-98, assuming that ground is in good condition)

7 PIN CONFIGURATIONS (Fig6, Tab4)

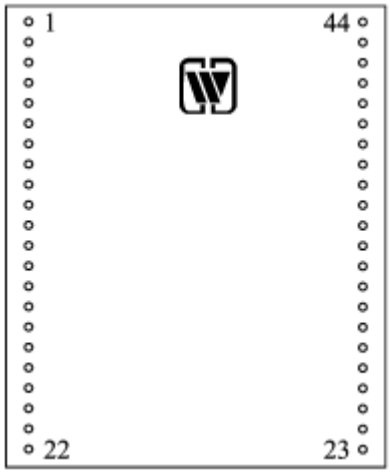


Figure 6 Pin out top view

Table 4 Pin description

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	A_{s3}	Fine channel input	23	case	Case ground
2	A_{s1}	Fine channel input	24	NC	Not connected
3	A_{s4}	Fine channel input	25	64:1MSB D1	Output of the highest combined digital angle
4	A_{s2}	Fine channel input	26	32:1MSB D2	Output of combined digital angle
5	B_{s1}	Coarse channel input	27	16:1MSB D3	Output of combined digital angle
6	B_{s3}	Coarse channel input	28	8:1MSB D4	Output of combined digital angle
7	B_{s4}	Coarse channel input	29	D5	Output of combined digital angle
8	B_{s2}	Coarse channel input	30	D6	Output of combined digital angle
9	T_1	Adjustment pin for phase shift	31	D7	Output of combined digital angle
		between signal and reference	32	D8	Output of combined digital angle
10	T_2	Adjustment pin for phase shift	33	D9	Output of combined digital angle
		between signal and reference	34	D10	Output of combined digital angle
11	SC1	Program control pin for coarse	35	D11	Output of combined digital angle
		and fine speed ratios	36	D12	Output of combined digital angle
12	SC2	Program control pin for coarse	37	D13	Output of combined digital angle
		and fine speed ratios	38	D14	Output of combined digital angle
13	R_{Hi}	Input pin for reference high	39	D15	Output of combined digital angle
14	R_{Lo}	Input pin for reference low	40	D16	Output of combined digital angle
15	Inhibit	Inhibit signal	41	D17	Output of combined digital angle
16	-15V	-15V input	42	D18	Output of combined digital angle
17	+15V	+15V input	43	D19	Output of combined digital angle
18	GND	ground	44	D20	Output of the least combined digital angle
19	+5V	+5V input			
20	$\overline{Enable_{Mi}}$	enable middle 8bits data			
21	$\overline{Enable_{Lo}}$	enable low 8bits data			
22	$\overline{Enable_{Hi}}$	enable high 4bits data			

Note: ① Pin3,7 of HTS20S are not connected.

② A_{s1},A_{s2}, A_{s3}, A_{s4} are fine channel input. If synchro is equipped with three wire, A_{s4} is not used.

③ B_{s1},B_{s2},B_{s3},B_{s4} are coarse channel input. If synchro is equipped with three wire, B_{s4} is not used.

④ R_{Hi}, R_{Lo} are reference signal input.

Inhibit is inhibit signal which is connected to 5V power supply by pull-up resistor. When $\overline{Inhibit}$ is logical "0", inside is inhibited. After 490ns, valid data are outputted and can be read. When $\overline{Inhibit}$ is logical "1", converter restores tracking state, the outputted data are invalid data.

$\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ are three state control pins of data output, which determined the state of outputted data. When they are logical "1", data output pin is in high impedance. When they are logical "0", After 200ns, data output pin outputs valid data. Outputted data state doesn't affect the loop operation inside converter. $\overline{Enable_{Lo}}$ controls low 8bits data, $\overline{Enable_{Mi}}$ controls middle 8bits data, $\overline{Enable_{Hi}}$ controls the rest high bits data.

T_1 and T_2 are phase shift adjustment network between coarse/fine channel signal and reference, circuit types are shown in figure7. By selecting R,C , it makes phase shift between signal and reference less than 10°.The type of R,C phase shift network can be adjusted according to advance and lag relation between signal and reference during test. If adjustment of phase shift is not needed, T1 and T2 are shorted out.

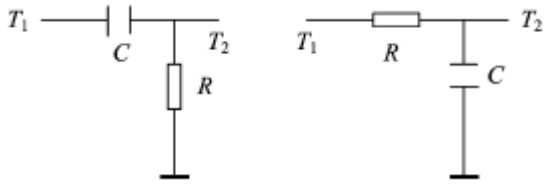


Figure 7 Phase shift adjustment network diagram

SC1,SC2 are speed ratio program control pins of coarse/fine channel. When used, they are connected to ground by 10kΩ or to +5V voltage. The truth table is:

SC1	SC2	Multipolar resolver speed ratio
0	0	1:8
0	1	1:16
1	0	1:32
1	1	1:64

Case is case pin.

D_1~D_{20} are Outputs of combined digital angle. D_{20} is least significant bit. When speed ratio is 1:8, D_4 is most significant bit. When speed ratio is 1:16, D_3 is most significant bit. When speed ratio is 1:32, D_2 is most significant bit. When speed ratio is 1:64, D_1 is most significant bit.

8 BIT WEIGHT TABLE (Tab 5)

Table 5 Bit weight table

Bit number	Weight (degrees)	Bit number	Weight (degrees)	Bit number	Weight (degrees)
1(MSB)	180.0000	8	1.1063	15	0.011(40sec)
2	90.0000	9	0.7031	16	0.0055(20sec)
3	45.0000	10	0.3516	17	0.00275(10sec)
4	22.5000	11	0.1758	18	0.00138(5sec)
5	11.2500	12	0.0879	19	6.88×10^{-4}(2.5sec)
6	5.6250	13	0.0439	20	3.44×10^{-4}(1.25sec)
7	2.8125	14	0.0220		

9 CONNECTION OF CONVERTER

±15V,+5V and ground are connected to the corresponding pins of the converter. Pay attention to the polarity of power supply, or it will harm device. It is suggested that 0.1μf and 6.8μf by-pass capacitors are connected between power supplies and ground.

Signal and exciting source are permitted to be connected to S_1,S_2,S_3,S_4 and R_{Hi} , R_{Lo} with 5% error.

Signal input should be in coordination with exciting phase, their phases are as follows:

R_{Hi} ~R_{Lo} :V_{Ref}sinωt

In the case of synchro:

S_1~S_3: $E_{S1\sim S3}=E_{RLo\sim RHi}\sin\theta\sin\omega t$

S_3~S_2: $E_{S3\sim S2}=E_{RLo\sim RHi}\sin(\theta+120°)\sin\omega t$

S_2~S_1: $E_{S2\sim S1}=E_{RLo\sim RHi}\sin(\theta+240°)\sin\omega t$

In the case of resolver:

S_1~S_3: $E_{S1\sim S3}=E_{RLo\sim RHi}\sin\theta\sin\omega t$

S_2~S_4: $E_{S2\sim S4}=E_{RHi\sim RLo}\cos\theta\sin\omega t$

Note: input signals in R_{Hi}, R_{Lo}, S_1, S_2, S_3, S_4 are not permitted to connect other pins, or it will damage the device.

Other pins should be connected according to pin definition of the device.

It is suggested that user should inform manufacturer to have device made to order according to parameters when using non-nominal synchro or resolver.

10 PACKAGE OUTLINE DIMENTION AND DISCRIPTION

(Unit: mm**) (** Fig 8, Tab 6 **)**

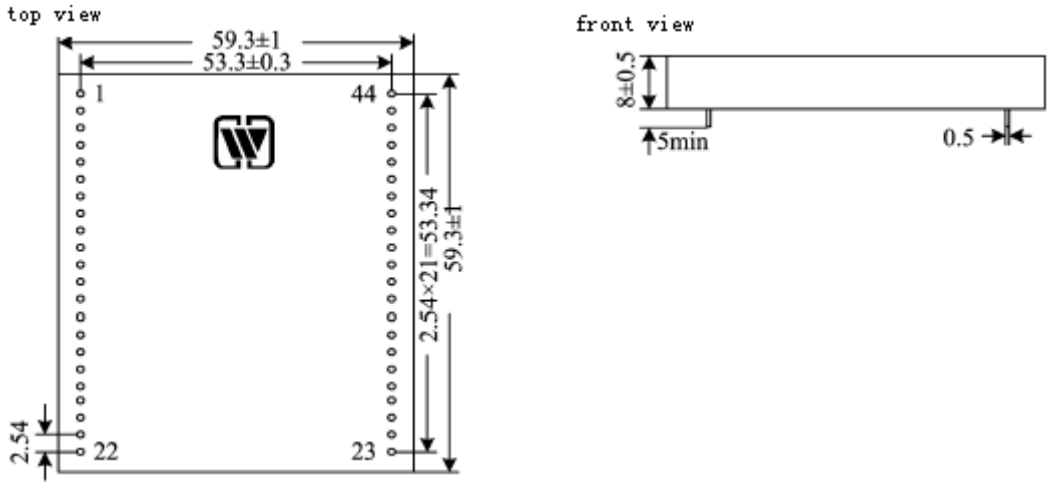


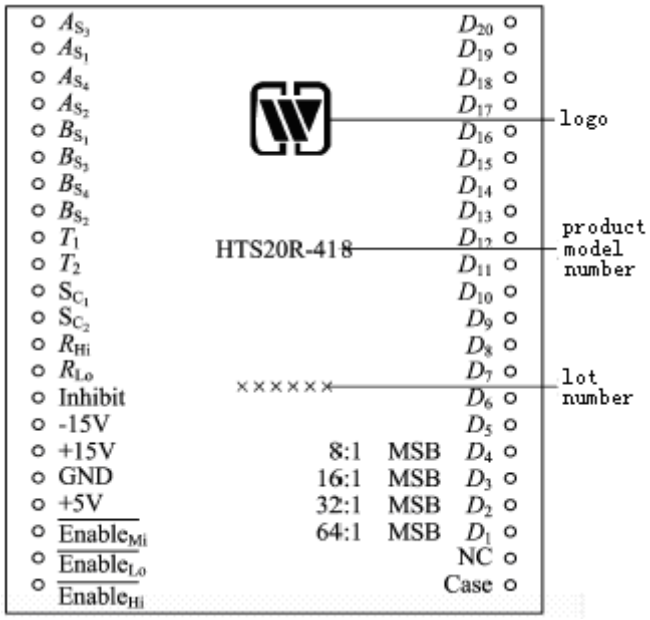
Figure 8 Package outline drawing

Table 6 Packaging case descriptions

Case model	Base material	Base coat	Lid(cap) material	Lid(cap) coat	Lead material	Lead coat	Sealing method	Comments
UP5959-44	Kovar (4J29)	Ni/Au	Fe/Ni alloy	Ni/Au	Kovar (4J29)	Ni/Au	Match sealing	

Note: The temperature of soldered pins does not surpass 300℃ within 10 sec.

11 DESCRIPTIONS OF PRODUCT MODEL NUMBERING (Fig 9)



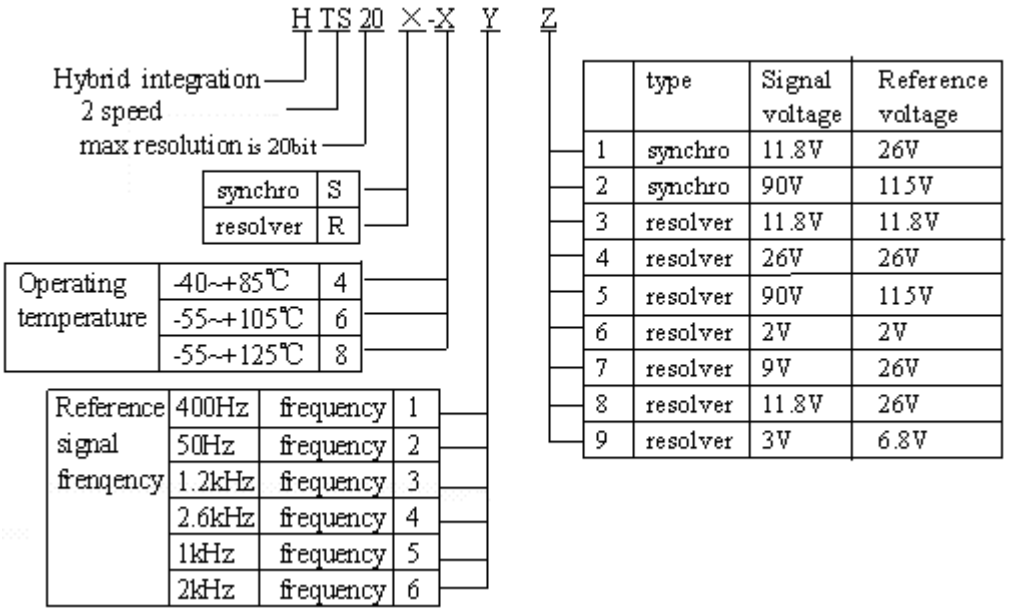
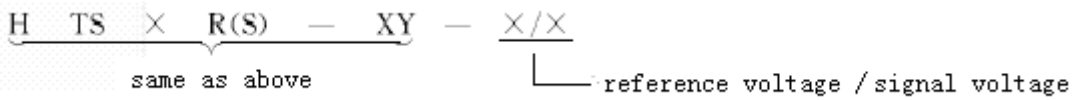


Figure9 Descriptions of product name

Note: When signal voltage and reference voltage(Z) above are not nominal, product name is given as follows:



(for example, reference voltage is 5V, signal voltage is 3V, name denotes 5/3)

Application notes:

★Polar voltage of power supply should be correct.

★When exceeding absolute maximum nominal value, it will possibly lead to damage to the device.

★While assembling, the bottom of the product should be placed close to the board to avoid damage to the pins. If necessary, take shockproof measures.

★When product is ordered, detailed electrical performance specifications should be referred to corresponding business standard.