Two-speed Modular SDC/RDC Converter (Series MTS)

1 FEATURES (Outline is shown in Fig 1. Classifications are shown in table1)

- Complete 2-speed system
- 1:64, 1:32,1:16, 1:8, 1:20, 1:36(optional)
- Digital output with 3-state latches
- Maximum resolution is 20 bit
- Maximum accuracy is 5 Arc sec

2 APPLICATIONS

- Radar
- Navigation
- Satellite tracking
- Artificial technology
- Artillery control
- Industrial machine control
- Other high-accuracy measurement

3 GENERAL DESCRI PTION

2-speed SDC/RDC converters(series MTS) are modular monolithic circuits. They internally contain coarse/fine two way function generator and processing circuit required by two speed system.

2-speed modular converters(series MTS) are classified as two types:

(1) 2-speed combined converter

(2) 2-speed continuous converter

Speed ratios of coarse/fine combination of 2-speed SDC/RDC converter(series MTS) products are arbitrary value between 1:2 and 1:64. Two way coarse/fine input signals are signals of three-wire synchro or four-wire resolver.

2-speed SDC/RDC converters(series MTS) output natural parallel binary codes. Maximum is up to 20bit. They have 3-state latches.

Size:79.4×66.7×18.5mm^3 (type A)
79.4×66.7×11.3mm^3 (type B)
Weight:190g(type A)
103g(type B)

Figure1 series MTS outline

Table1 Product classification

Synchro	Resolver
MTS36S-412	MTS19R36-418 (MTS36R-418)
MTS16S-412	MTS36R-467

4 TECHNICAL SPECIFICATIONS (Tab 2, Tab 3)

Table2 Nominal conditions and recommended working conditions

Absolute max nominal value	Power supply voltage Vs:±17V 5V power supply voltage V_L:7V Storage temperature range:-55~+105℃
Recommended working conditions	Power supply voltage +Vs: 15V±0.75V Power supply voltage -Vs: -15V±0.75V 5V power supply voltage V_L: 5V±0.25V Reference voltage(effective value)V_{Ref}:2～115V Signal voltage(effective value)V_I: 2～90V Reference frequency f : 50～10kHz Operating temperature range T_A: -55~+105℃

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Table3 Electrical characteristics

Characteristics	Conditions	Series MTS Business military standard (Q/HW30945-2006)	
		Min	Max
Resolution(bit)	speed ratio 1:8	-	17
	speed ratio 1:20	-	18
	speed ratio 1:36	-	19
	speed ratio 1:64	-	20
Accuracy(sec) (range 0 ° ~360 °)	speed ratio 1:8	-	40
	speed ratio 1:20	-	20
	speed ratio 1:36	-	10
	speed ratio 1:64	-	5
Tracking velocity in fine channel/rev/s	400Hz	-	36
Frequency/Hz	-	50	10000
Exciting voltage(effective value)/V	-	2	115
Signal voltage(effective value)/V	-	2	90
Power dissipation/W	±15V,+5V	-	2.5

5 PRINCIPLES OF OPERATING

（1）2-speed combined converter

The principle of operation of 2-speed combined converter is shown in fig2. The operation of the coarse and fine channel of the 2-speed converter is the same as above-mentioned single speed converter, but 2-speed converter consists of two sets of single speed converter and programmer error-correcting logical circuit. Coarse channel fulfills conversion from 10~12bit logical angle to digital angle. Fine channel fulfills conversion from 14bit logical angle to digital angle. digital angles converted by Coarse channel and Fine channel are inputted into programmer error-correcting logical circuit respectively. After error processing and correcting, it will output a 20bit parallel binary digit, which is inputted into output latch and buffered to output digital angle, fulfilling the entire conversion.

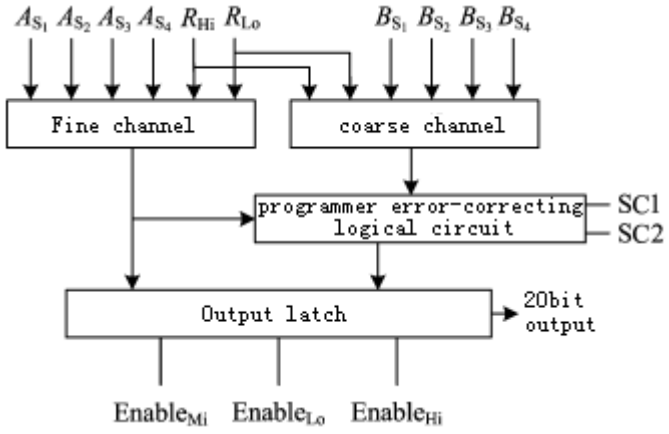

Figure2 Functional block diagram of 2-speed combined converter

(2) 2-speed continuous converter

2-speed continuous converter has two sets of coarse and fine error signal-generating circuits. The two sets are controlled by one up/down counter. Cross detector selects one of two coarse and fine error signals to integrate according to error signal value of coarse axis, controls VCO, makes

counter count and 3-state latch output. Its principle of operation is shown in fig3.

The series mainly consist of the following parts: ① interface circuit, ② data processing circuit, ③ function generator circuit, ④ cross detector circuit, ⑤ false zero cancel circuit, ⑥ synchro reference circuit, ⑦ 20 bit counter.

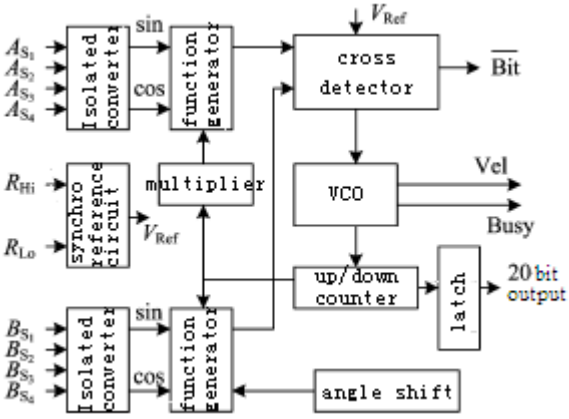

Figure3 Functional block diagram of 2-speed continuous converter

Synchro/resolver signals from coarse channel and fine channel are inputted into analog signal input pin of continuous SDC/RDC converter respectively(signal with original multiple is inputted into coarse channel, signal with 36 bit is inputted into fine channel). After conversion by converter, latch outputs binary codes(maximum is up to 20bit) which represent angles.

(3)data transfer method and timing

Outputs of series MTS 2-speed converters reach 20bit. Through $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ which take 3-state control of output latch, 2-speed converter can be easily connected to data bus. $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ are all valid at low level. $Enable_{Lo}$ controls low 8bits, $Enable_{Mi}$ controls middle 8bits, $Enable_{Hi}$ controls rest high bits.

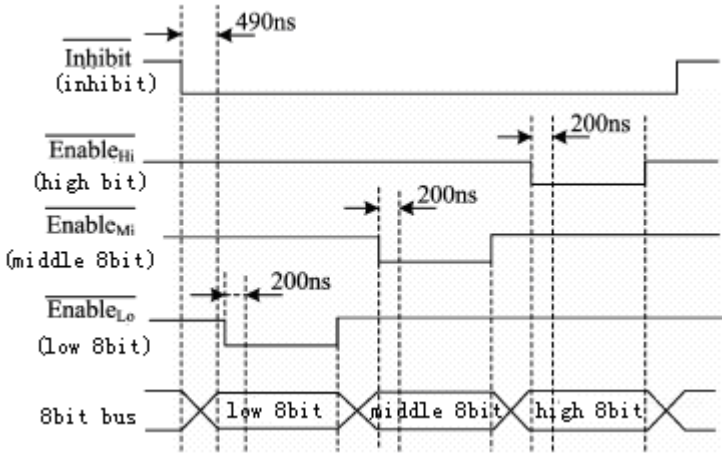

Figure 4 Timing diagrams during 8bit bus transmission

Data of series MTS 2-speed converters are read as follows: Set Inhibit to logical "0", lock valid data of converter, after 490 μ m, It can read data of low 8bits, middle 8bits and high bits through controlling $Enable_{Lo}$, $Enable_{Mi}$ and $Enable_{Hi}$. Figure 4 gives timing of reading data when 2-speed converter and 8 bit data bus are connected.

To ensure high-accuracy conversion of 2-speed converter, please pay attention to the following:

① errors of input signal voltage of coarse and fine channels should be guaranteed within 10% of nominal value.

② Frequencies of input signals and reference signals of coarse and fine channels should be within the specified operating frequency range.

③ If select 2-speed combined converter :

(a) Phase shift between input signal and reference signal of coarse channel should be less than 10°.

(b) phase shift between input signal and reference signal of fine channel should be less than 10°.

④ Wave distortions of input signals and reference signals of coarse and fine channels should be less than 10%,

⑤ Variation of +5V, ±15V power supply voltage should be guaranteed within ±5%.

6 MTBF DIAGRAM (Fig 5)

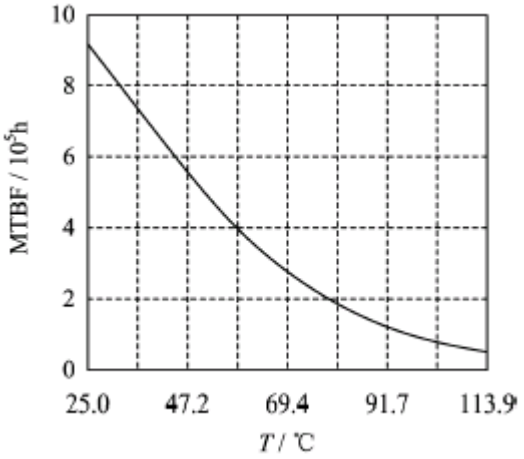

Figure 5 MTBF vs. temperature

7 PIN CONFIGURATIONS (Fig6, Tab4)

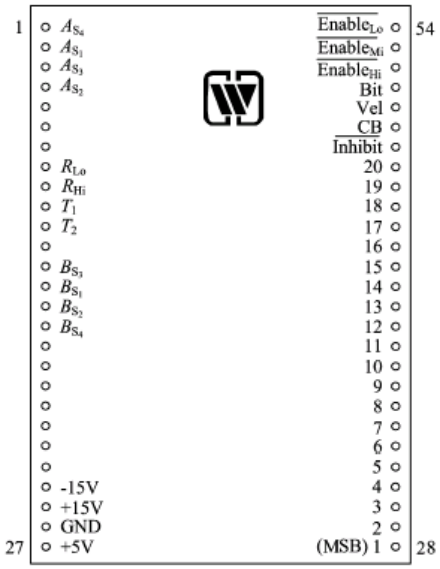

Figure 6 Pin out top view

(Note: According to GJB/Z 299B-98, assumingthat ground is in good condition)

Table 4 Pin description

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	A_{S4}	Fine channel input	35	D_8	Data output 8th bit
2	A_{S1}	Fine channel input	36	D_9	Data output 9th bit
3	A_{S3}	Fine channel input	37	D_{10}	Data output 10th bit
4	A_{S2}	Fine channel input	38	D_{11}	Data output 11th bit
8	R_{Lo}	Exciting input low	39	D_{12}	Data output 12th bit
9	R_{Hi}	Exciting input high	40	D_{13}	Data output 13th bit
10	T_2	Pin for phase shift between	41	D_{14}	Data output 14th bit
		signal and reference	42	D_{15}	Data output 15th bit
11	T_1	Pin for phase shift between	43	D_{16}	Data output 16th bit
		signal and reference	44	D_{17}	Data output 17th bit
13	B_{S3}	Coarse channel input	45	D_{18}	Data output 18th bit
14	B_{S1}	Coarse channel input	46	D_{19}	Data output 19th bit
15	B_{S2}	Coarse channel input	47	D_{20}	Low data output 20th bit
16	B_{S4}	Coarse channel input	48	Inhibit	Inhibit pin
24	+15V	+15V power supply	49	CB	Busy output pin
25	-15V	-15V power supply	50	Vel	Velocity output pin
26	GND	Ground	51	Bit	Bit signal output
27	+5V	+5V power supply	52	$Enable_{Hi}$	High 3bit enable pin
28	(MSB)D_1	High data output 1st bit	53	$Enable_{Mi}$	Middle 8bit enable pin
29	D_2	High data output 2nd bit	54	$Enable_{Lo}$	Low 8bit enable pin
30	D_3	Data output 3rd bit			
31	D_4	Data output 4th bit			
32	D_5	Data output 5th bit			
33	D_6	Data output 6th bit			
34	D_7	Data output 7th bit			

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Note: ① A_{s1},A_{s2}, A_{s3},A_{s4} are fine channel input. If synchro is equipped with three wire, A_{s4} is not used.

② B_{s1},B_{s2},B_{s3},B_{s4} are coarse channel input. If synchro is equipped with three wire, B_{s4} is not used.

③R_{Hi}, R_{Lo} are reference signal input.

④$\overline{Inhibit}$ is inhibit signal which is connected to 5V power supply by pull-up resistor. When $\overline{Inhibit}$ is logical "0", inside is inhibited. After 490ns, valid data are outputted and can be read. When $\overline{Inhibit}$ is logical "1", converter restores tracking state, the outputted data are invalid data.

⑤$\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ are three state control pins of data output, which determined the state of outputted data. When they are logical "1", data output pin is in high impedance. When they are logical "0", After 200ns, data output pin outputs valid data. Outputted data state doesn't affect the loop operation inside converter. $\overline{Enable_{Lo}}$ controls low 8bits data, $\overline{Enable_{Mi}}$ controls middle 8bits data, $\overline{Enable_{Hi}}$ controls the rest high bits data.

⑥T1 and T2 (2-speed continuous converter does not need T1 and T2 due to internal phase self-adaptive circuit)are phase shift adjustment network between fine channel signal and reference, circuit types are shown in figure7. By selecting R,C , it makes phase shift between signal and reference less than 10°.The type of R,C phase shift network can be adjusted according to phase advance and phase lag relation between signal and reference during test. If adjustment of phase shift is not needed, T1 and T2 are shorted out.

⑦Vel is fine channel velocity signal

⑧D_1~D_{20} are Outputs of combined digital angle. D_1 is most significant bit. D_{20} is least significant bit.

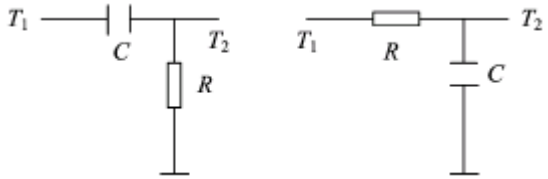


Figure7 Phase shift adjustment network diagram

8 BIT WEIGHT TABLE (Tab 5)

Table 5 Bit weight table

Bit number	Weight (degrees)	Bit number	Weight (degrees)	Bit number	Weight (degrees)
1(MSB)	180.000 0	8	1.106 3	15	0.011(40sec)
2	90.000 0	9	0.703 1	16	0.005 5(20sec)
3	45.000 0	10	0.351 6	17	0.002 75(10sec)
4	22.500 0	11	0.175 8	18	0.001 38(5sec)
5	11.250 0	12	0.087 9	19	6.88×10^{-4}(2.5sec)
6	5.625 0	13	0.043 9	20	3.44×10^{-4}(1.25sec)
7	2.812 5	14	0.022 0		

9 CONNECTION OF CONVERTER

±15V, 5V and ground are connected to the corresponding pins of the converter. Pay attention to the polarity of power supply, or it will harm device. It is suggested that 0.1μf and 6.8μf by-pass capacitors are connected between power supplies and ground.

Signal and exciting source are permitted to be connected to S_1,S_2,S_3,S_4 and R_{Hi} , R_{Lo} with 5% error.

Signal input should be in coordination with exciting phase, their phases are as follows:

R_{Hi} ~R_{Lo} :V_{Ref}sinωt

In the case of synchro:

S_1~S_3: $E_{S1\sim S3}=E_{RLo\sim RHi}\sin\theta\sin\omega t$

S_3~S_2: $E_{S3\sim S2}=E_{RLo\sim RHi}\sin(\theta+120°)\sin\omega t$

S_2~S_1: $E_{S2\sim S1}=E_{RLo\sim RHi}\sin(\theta+240°)\sin\omega t$

In the case of resolver:

S_1~S_3: $E_{S1\sim S3}=E_{RLo\sim RHi}\sin\theta\sin\omega t$

S_2~S_4: $E_{S2\sim S4}=E_{RHi\sim RLo}\cos\theta\sin\omega t$

Note: input signals in R_{Hi}, R_{Lo}, S_1, S_2, S_3, S_4 are not permitted to connect other pins, or it will damage the device.

Other pins should be connected according to pin definition of the device.

It is suggested that user should inform manufacturer to have device made to order according to parameters when using non-nominal synchro or resolver.

10 PACKAGE OUTLINE DIMENTION AND DISCRIPTION(Unit: mm) (Fig 8)

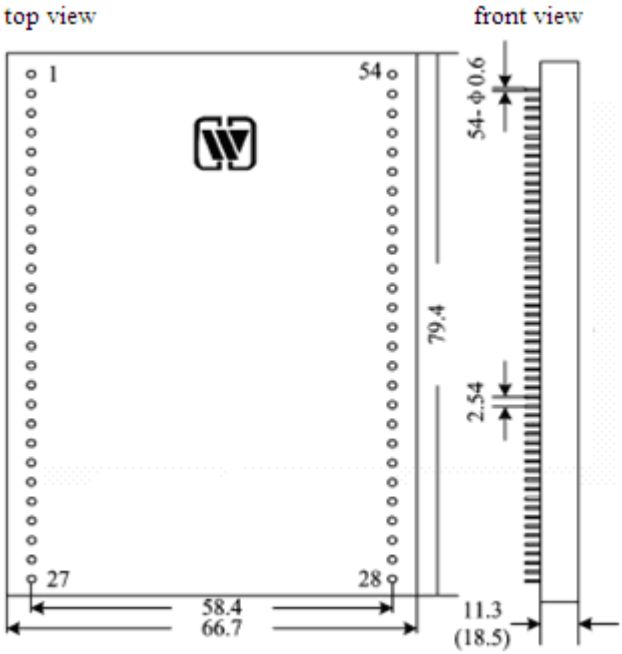


Figure 8 Package outline drawing

11 DESCRIPTIONS OF PRODUCT MODEL NUMBERING (Fig 9)

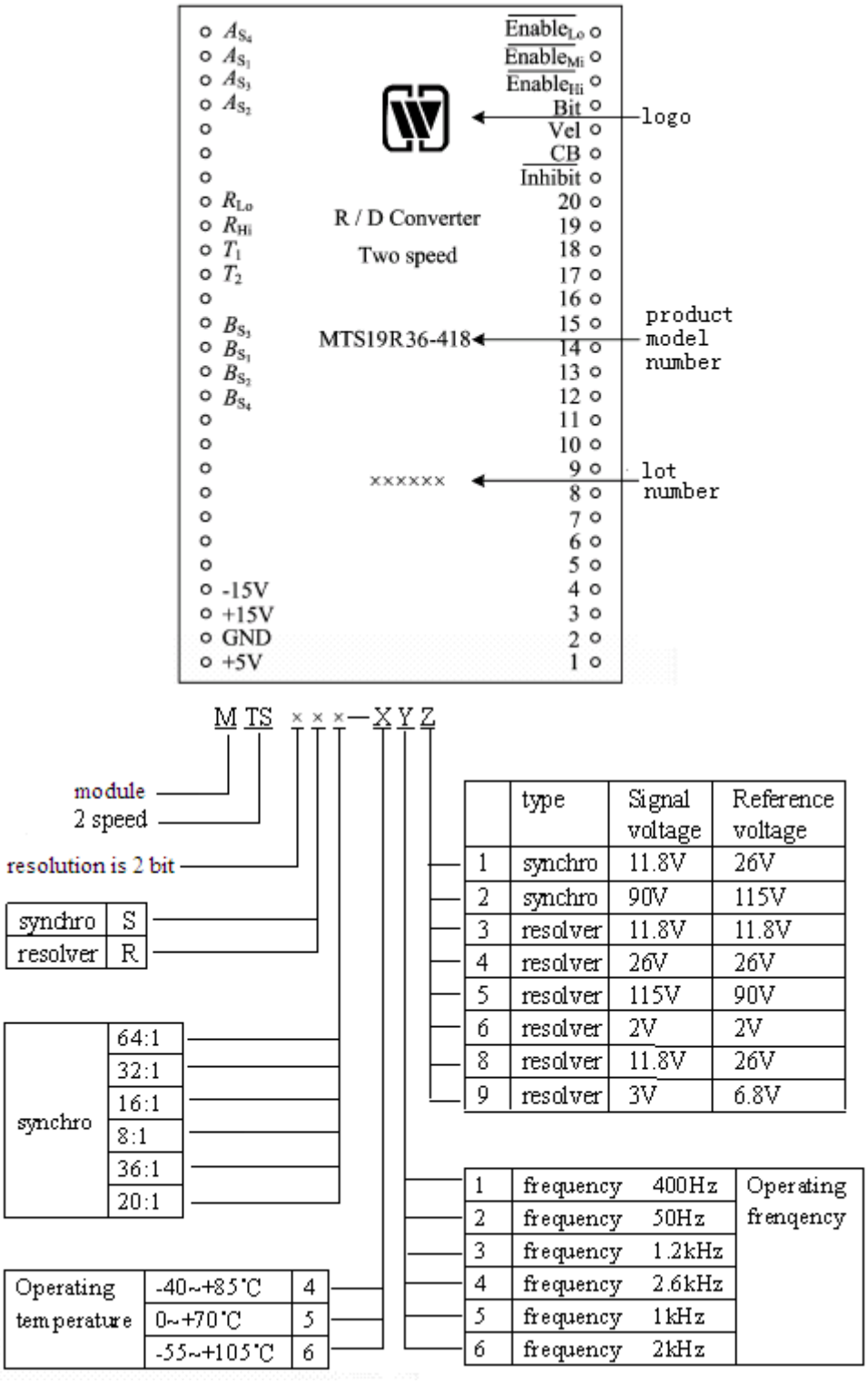
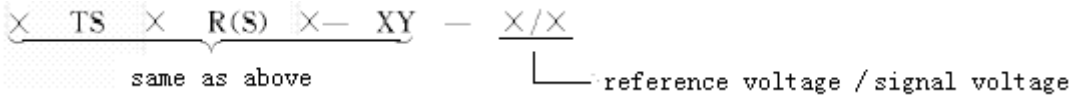


Figure 9 Descriptions of product name

Note: When signal voltage and reference voltage(Z) above are not nominal, product name is given as follows:



(for example, reference voltage is 5V, signal voltage is 3V, name denotes 5/3)

Application notes:

★Polar voltage of power supply should be correct.

★When exceeding absolute maximum nominal value, it will possibly lead to damage to the device.

★While assembling, the bottom of the product should be placed close to the board to avoid damage to the pins. If necessary, take shockproof measures.

★When product is ordered, detailed electrical performance specifications should be referred to corresponding business standard.