The design of the two-speed digital to resolver converter with coarse-fine combination

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Abstract: According to the multi-polar resolver to digital converter's combination of coarse -fine axis angle and its error correction, this paper presented a two-speed digital to resolver converter with coarse-fine combination. Based on RD-19230 and CPLD, the two-speed digital to resolver converter is equipped to finish the coarse-fine data transformation, combination and correction, which meets the two-speed digital to resolver converter's requirements of high accuracy and miniaturization.

1 Introduction

As the numerical control system aim to the high accuracy and high integration level, the resolver to digital converter has new requirements.

1. High accuracy: The resolver to digital converter using multi-polar converter as the angular transducer is called two-speed converter. The application of the combination of coarse-fine axis angle can increase the measuring precision of the two-speed converter.
2. High integration level: The two-speed digital to resolver converter with coarse-fine combination is composed of synchronous and corrective logic circuit which means two-speed logic processor. The two-speed logic processor is coming from the combination and correction of two single-speed converters and data using in the coarse-fine channel transformation. The two-speed digital to resolver converter's miniaturization is finished by optimizing and designing the single-speed converter and two-speed logic processor.

2 The design principle

2.1 The operating principle of the two-speed digital to resolver converter

The resolver signal from the fine axis angle θ_f transforms into digital angle Φ_f through the resolver to digital converter. The resolver signal from the coarse axis angle θ_c transforms into digital angle Φ_c through the resolver to digital converter. These two digital angles output 20 bits parallel binary digit to the latch through the coarse-fine combination and correction of the two-speed processor to complete the whole transformation. The operating principle of the two-speed digital to resolver converter with coarse-fine combination is shown in the figure 1 below:

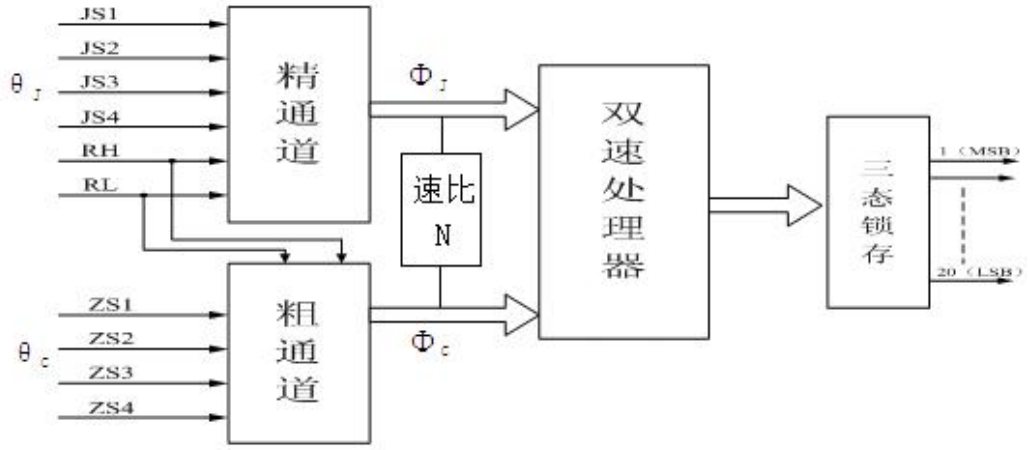

Figure 1 The operating principle of the two-speed digital to resolver converter with coarse-fine combination

2.2 The combination of coarse and fine axis angle

When the coarse-fine speed ratio of multi-polar digital to resolver converter is 1: N, the coarse axis angle Φ_c runs on a 360^o cycle and the fine axis angle Φ_j runs on a $360^o/N$ cycle. That means if the coarse axis angle Φ_c rotates by a full turn, the fine axis angle Φ_j rotates by N turns.

If the speed ratio is $N=2^m$, and two converters have same bits, then the coarse-fine axis angle's weight coefficients of every output numerical codes have the corresponding relations below:

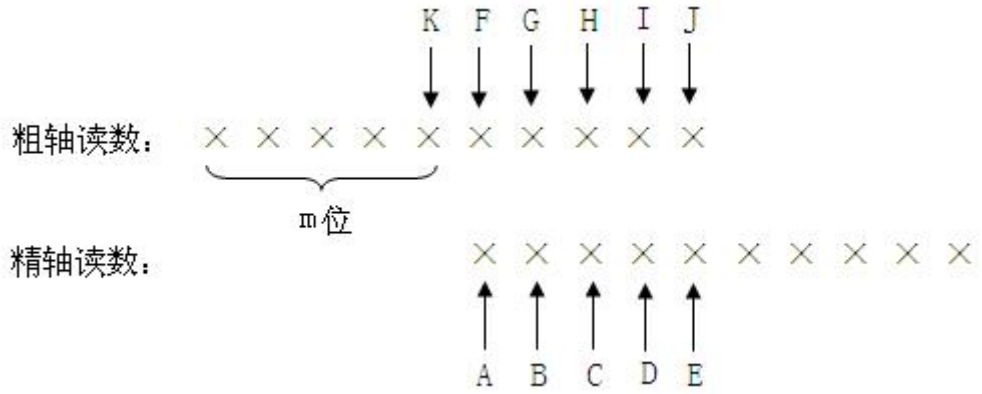

Figure 2 The relationship between the coarse-fine combinations

Ideally, the coarse-fine readings' overlaps F~J and A~E should have been the same. When the fine axis angle takes a turn, the coarse axis angle's reading K should plus 1. So the coarse axis angle's top m readings represent the whole cycles which the fine axis angle turns. The coarse-fine combination's reading system is coming from arranging and outputting the coarse axis angle's top m readings and whole fine axis angle readings in turns.

So the principle of the random speed ratio of the coarse-fine data combination is:

If Φ_c is integer part representing the cycles fine axis angle turns and Φ_J is decimal part, then:

$[\Phi_c]$ integer part $=INT[\Phi_c \times N/360^\circ] \times (360^\circ/N)$; （1）

$[\Phi_J]$ decimal part $=\Phi_J/N$。 （2）

So the axis angle after combining is

Φ=[Φ_c] integer part + Φ_J/N

=INT[Φ_c /360° /N]×(360° /N)+ Φ_J/N （3）

The based thought of the coarse-fine combination is amplifying the speed ratio and measuring for attaining the goal of increasing the accuracy. For example, when the actual axis angle Φ=203.5°, and if the single polar resolver to digital converter's accuarcy of measurement is 1º, then the integer part 0.5º cannot be measured. But after combining the coarse-fine axis angles, the coarse axis angle Φ_c is actually 203.5º . If the speed ratio is 1:36, with the formula (1), the Φ_c's integer part is INT[203.5° ×36/360] ×（360° /36）=200° , the Φ_J's fine axis angle reading is 203.5°×36-INT[203.5°×36/360]×360°=126°. Because it is a result amplified 36 times, so result should be reduced 36 times with the coarse-fine combination. Due to the formula (2), the Φ_c's integer part is 126°/36=3.5°. so the coarse-fine combination reading is 200°+3.5°=203.5°.

2.3 The correction of coarse and fine axis angle

The coarse-fine combination shown above is based on no wrong coarse axis angle. However, due to transmission error, multi-polar resolver error and axis angle error, the precise match between coarse and fine axis angles is impossible, so that the coarse anix angle reading has one more number 1 or has one less number 1. Thus, the coarse-fine anix angles have to be correct when they are combinating. The principle of correcting is using fine axis angle to correct coarse axis angle.

There are 3 conditions:

(1) When the fine axis angle is in the first quartile, the coarse one only needs slightly count rather than largely count. As the figure 2 showing, when the fine axis angle data is overflowing, we should carry in 1 at coarse axis angle's data K. But the coarse axis angle's mantissa may not carry bit to the fifth bit, at that time we must correct that carry in 1 at coarse axis angle's data K.

(2) When the fine axis angle is in the fourth quartile, the coarse one only needs largely count rather than slightly count. As the figure 2 showing, when the fine axis angle data hasn't overflowed, we shouldn't carry in 1 at coarse axis angle's data K. But the coarse axis angle's mantissa carry bit to data K, at that time we must correct that carry out 1 at coarse axis angle's data K.

(3) When the fine axis angle is in the second and third quartiles, the coarse one has no carry bit. So the coarse axis angle doesn't have to correct due to impossibility of counting more or less.

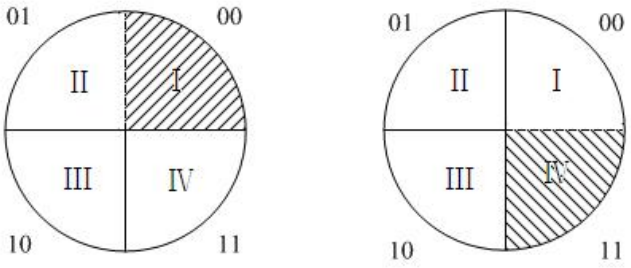

Figure 3 The relationship between the partition of fine axis angle's quartile and its top two readings

3 The circuit design

3.1 The design of coarse and fine converter

The design of coarse and fine converters regards the RD-19230 as the key design. RD-19230 is a highly reliable and general monolithic integration circuit of resolver to digital converter with advantages of resolution ratio, programmable velocity voltage, double bandwidth, high accuracy, low power dissipation and small volume. It needs concise peripheral circuit to realize the transformation between the coarse and fine combination.

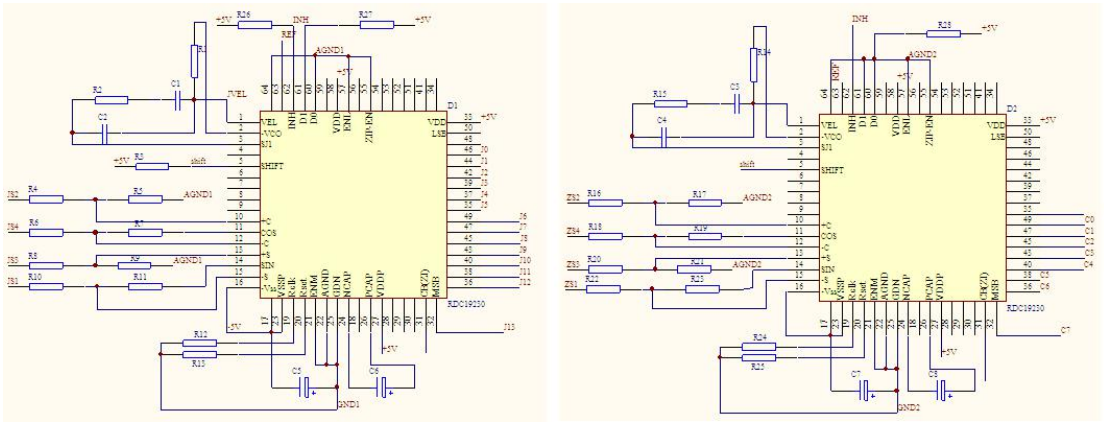

Figure 4 The schematic diagram of the coarse and fine converter based on coarse and fine converter

From the figure 4 we can see that the operating principle of the coarse converter is the same as fine converter's. Due to the correction of coarse and fine combination and indexes of actual products, we have to respectively design coarse and fine converters. The main differences are: 1) resolution ratio; 2) close loop parameters such as tracking speed rate and width.

1) Choosing resolution ratio

The formula of the outputting angle of the coarse and fine converters is:

$\Phi=[\Phi_C]$ integer part $+\Phi_J/N=INT[\Phi_C/360°/N]\times(360°/N)+\Phi_J/N$

The coarse axis angle reading represents whole rounds that fine integer part cycles. So we choose high several significance bits of the coarse axis angle for its low significance bits are less accurate than fine axis angle amplifying N times. The speed ratio of two-speed converter is 1:36. The precision is ±10 second of arc. So the fine channel's conversion accuracy r is required to be ±10×36/60=±6 minute of arc. The accuracy of single speed converter with 14 bit resolution ratio is ±5.3 minute of arc. So in the design, the fine channel's conversion accuracy is 14 bit while the coarse channel's conversion accuracy is 12 bit.

2) Designing close loop parameters

The converter's transfer function shown in the figure 5 reveals that for 14 bit and 12 bit single speed converter, the key point is choosing width and tracking speed.

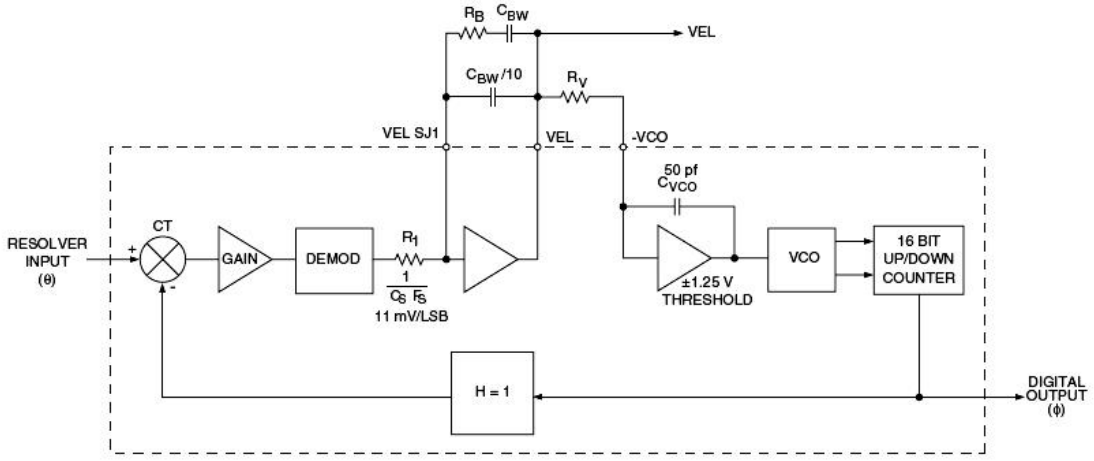

Figure 5 The converter's transfer function

In the figure, C_{BW} decides fine channel converter's bandwidth, R_V decides converter's max tracking speed RPS. Decreasing bandwidth will increase converter's stability and uneasily make low flash. But excessively wide bandwidth will influence max tracking speed. The chart 1 shows the relationship between the resolution ratio converter's tracking speed ratio and bandwidth's ratio.

The chart 1 The relationship between the resolution ratio converter's tracking speed ratio and bandwidth's ratio

tracking speed ratio / bandwidth's ratio	
max tracking speed / bandwidth	resolution ratio
1	10
0.50	12
0.25	14
0.125	16

For 14 bit fine channel converter, the ratio between max tracking speed and bandwidth is:

$$\text{RATIO} = \frac{RPS}{BW} \leqslant 0.25,$$

For 12 bit coarse channel converter, the ratio between max tracking speed and bandwidth is:

$$\text{RATIO} = \frac{RPS}{BW} \leqslant 0.5.$$

$$\text{Rv} = \frac{VEL}{\text{max tracking speed (rps)} \times 2^{16} \times 50\,\text{pF} \times 1.25\,\text{V}},$$

$$C_{BW}\ (\text{pF}) = \frac{3.2 \times \text{Fs (Hz)} \times 10^{8}}{\text{Rv} \times (f_{BW})^{2}}。$$

In the formula, VEL is max velocity voltage and the converter's voltage is 4V. Fs is converter's inner sampling frequency 67 KΩ.

Based on the no influence in product's accuracy, theoretical calculation, analog simulation and dynamic parameter from the test optimization, choosing rational bandwidth and ensure max tracking speed ratio can make product's dynamic performance parameter doubtless and fine channel's rotated speed 32 rps.

3.2 The design of two-speed logic processor coarse and fine converters

The two-speed processor of multi-polar resolver to digital converter's coarse-fine combination relies on high-speed and high-performance digital device. The programmable logic device is characterized as high speed, large scale, programmable with powerful EDA. It is suitable to realize the technology of the two-speed processor of multi-polar resolver to digital converter. The design uses MAX II's EPM570T100I5 and the design tool is Altera's Quartus II. The VHDL is used in the whole circuit.

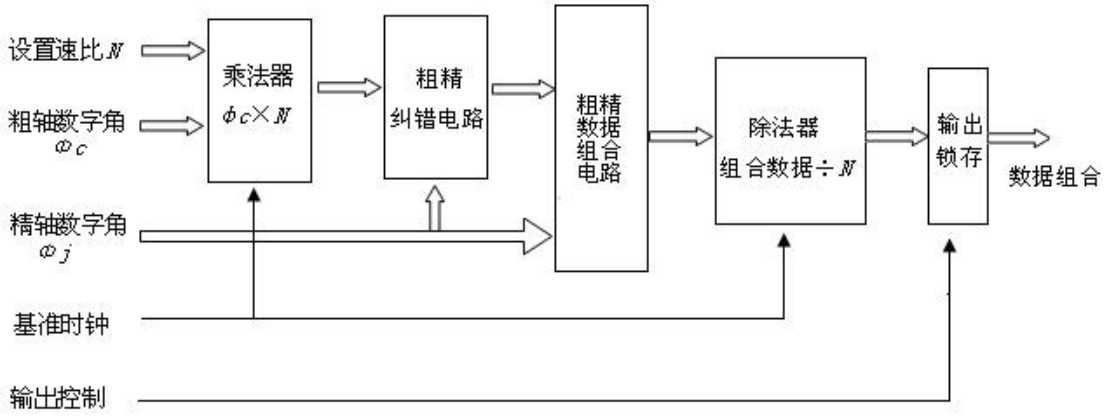

Figure 6 The principle of the two-speed processor

Using the programmable logic device to design two-speed processor has the key technical problem: Speeding up. The quality of the multiplier and divider directly influence two-speed processor's speed.

1) Design of the multiplier

The multiplication is one of the base operation applying widely digital signals. There are many ways to using the multiplier whose easiest way is using *. But this way cannot meet the requirement of the multiplication rate.

Two binary numbers multiply with formulation show that multiplication is finally formed with addition and shift operation. So we can use high-speed addition and shift operation to realize multiplication. For example, $N=36=2^5+2^2$ is fixed ratio, and we can make coarse channel data move 5 bit to the left and make later two data move 2 bit to the left. Then they plus together that means making coarse axis angle larger than 36 times.

After weighting, the coarse axis angle combines with fine coarse axis angle, and the low channel data is replaced with fine coarse axis angle. In the coarse axis angle's weighting circuit, the low channel data doesn't combine with coarse-fine data. So when we multiplying the coarse axis angle by speed ratio, decreasing the coarse axis angle's bits and multiplying the coarse axis angle's top 8 bits digital angles by speed ratio can save so many time.

The multiplier's source programs are:

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.std_logic_unsigned.ALL;
```

```
ENTITY RDC36 IS
PORT(clk_in : in std_logic;
        c_data : in std_logic_vector(7 downto 0)
c_inter36: out std_logic_vector(13 downto 0));
END RDC36;
ARCHITECTURE behave OF RDC36 IS
signal c_inter_5 : std_logic_vector(13 downto 0);
signal c_inter_2 : std_logic_vector(9 downto 0);
   begin
     c_inter_5 <= "0"&c_data(7 downto 0)&"00000";
     c_inter_2 <= c_data(7 downto 0)&"00";
     c_inter36 <= c_inter_5+c_inter_2;                    --c_data*36
```

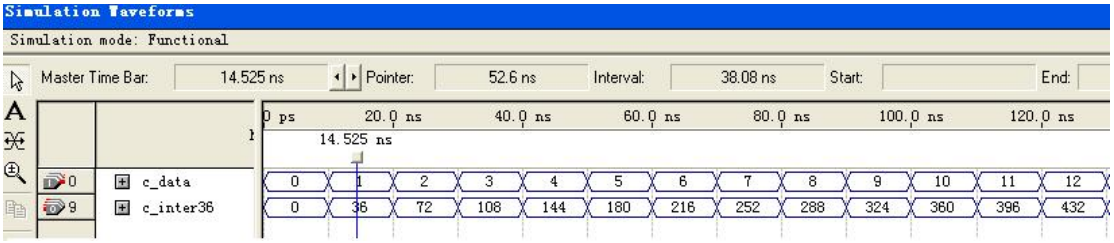

Figure 7 The simulation diagram of the multiplier

From the simulation diagram, we can see that it is a right result when we multiplying the coarse axis angle's top 8 bits digital angles by speed ratio N (36) means it amplifies 36 times. The design of the multiplier above completely meets the actual requirements.

2) Design of the divider

The divider circuit uses lpm_divide to start the division with segmenting integer and remainder. And for increasing the computational speed of the whole circuit, the divider uses pipelining that means divide the logic operation finished in one hour into several steps and add some clock periods to increase system's data throughout rate. That can drastically improve system's speed. The figure 8 is the simulation diagram of the divider.

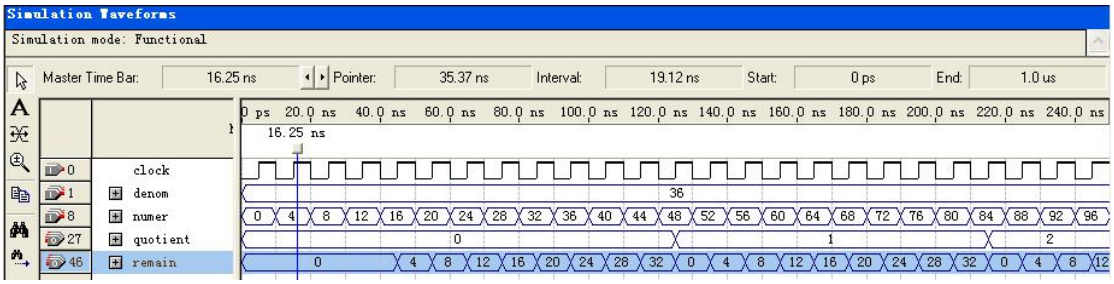

Figure 8 The simulation diagram of the divider

According to the simulation diagram, we divide the coarse-fine data amplified to 36 times by the speed ratio N (36) and get two-speed resolver to digital converter's actual output digital angle. And the result is right. The design of the divider above completely meets the actual requirements.

3) The analysis of the realizing the two-speed processor' with CPLD

Based on CPLD, we realize the two-speed processor circuit with coarse-fine speed ratio 1:36. And when the processor outputs 19 bits data, the circuit's max frequency is about 30 MHz. the figure 9 is analysis of the performance and figure 10 is the occupancy of resources.

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From
1	Worst-case tsu	N/A	None	7.142 ns	c_data[1]
2	Worst-case tco	N/A	None	25.265 ns	LPM_36:inst1|lpm_divide
3	Worst-case tpd	N/A	None	7.422 ns	JBUZY
4	Worst-case th	N/A	None	-1.069 ns	j_data[5]
5	Clock Setup: 'clk'	N/A	None	26.01 MHz (period = 38.447 ns)	LPM_36:inst1|lpm_divide
6	Total number of failed paths				

Figure 9 The analysis of the performance

Flow Summary

Flow Status	Successful - Tue Apr 08 16:39:11 2014
Quartus II Version	9.0 Build 132 02/25/2009 SJ Full Version
Revision Name	RDC19_36
Top-level Entity Name	RDC19_36
Family	MAX II
Device	EPM570T100I5
Timing Models	Final
Met timing requirements	Yes
Total logic elements	352 / 570 (62 %)
Total pins	48 / 76 (63 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

Figure 10 The occupancy of resources

Based on CPLD, the two-speed processor circuit with coarse-fine speed ratio 1:36 we realize though has large scale of hardware and low computational, it finish the combination and correction of the coarse-fine data with non-binary speed ratio. Compared with current two-speed processor with ROM chips, it has smaller volume that can complete miniaturization and change CPLD's inner circuit for suiting the two-speed system with different speed ratios.

4 Conclusions

Based on chips RD-19230, the coarse-fine two-speed converter with speed ratio 1:36 has higher accuracy than single speed converter. And the two-speed with programmable logic device CPLD uses VHDL to finish the whole circuit. It has advantages such as small volume, simple circuit and good practicability that suitable from every two-speed resolver to digital converters to digital-resolve system, which has wide applications.

Reference

[1] Xu Da-lin, Gao Wen-zhen, *The Multi-polar digital to resolver Converter with Coarse-fine Combination Based on FPGA*. Measurement and control technology, 2006,25,5.

[2]Wang Han-yi, *Analog-digital and Digital-analog Conversion Technology*. Harbin College of shipbuilding engineer press. Page 245-248.

[3] Wang Cheng, Wu Ji-hua. Altera FPGA/CPLD (Basic). Posts &Telecom Press. Page 1.