DC/DC Converter (MV24A Series)

1 Features

- Input voltage range: 18～36V
- Typical input voltage: 24V
- Output voltage: 3.3V,5V,12V,15V,24V,28V
- Input under-voltage lockout
- Output over-voltage protection
- Fault alarm
- Output voltage regulation range: 10%～110%
- Logical shutdown function
- ZCS/ZVS power structure, PFM control
- Can parallel and expand current, Accept N+M fault-tolerance model
- 3000V voltage isolation

57.9×55.9×12.70mm^3

weight≤30g

table 1 product category

MV24A3V3M264B MV24A5M400B MV24A12M400B	
MV24A15M400B MV24A24M400B MV24A28M400B	

2 Scope of application

For military and civil high reliability electronic systems in aviation, aerospace, vessel, armament, radar, railway, etc.

3 Descriptions

MV24C series DC/DC converter use ZCS/ZVS soft switching structure with low noise PFM control. The operating frequency can reach 1MHz. The pins can be replacement with similar products of VICOR. These products isolated 3000V voltage. The efficiency is up to 88% and power density is 80W/in3. The features of those products also include input over/under voltage lockout, output over-voltage protection and output over-current protection.

The design and production of products satisfy the requirements of SJ20668-1998 <microcircuit module standard> and product specifications (Q/HW32230-2013).

4 Technical Specificationss

Table 2: Rated conditions and Operating conditions

Absolute maximum rating	Operating conditions
+In -In Voltage：-0.5V～53V； PC -In Voltage：-0.5V～7.0V； PR -In Voltage：-0.5V～7.0V； SC -Out Voltage：-0.5V～1.5V； Storage temperature: -65～125℃ Welding temperature: (manual welding) (wave soldering)	Input voltage: 18～36V Working temperature （Tc）：-55～100℃

表 3 电特性 table 3(a) electrical characteristics

No.	Character		Symbol	Conditions （ Unless otherwise specified ，-55℃≤T_c≤125℃，V_{IN}=28V±5%）	MV24A3V3M264B		MV24A5M400B		MV24A12M400B	
					Min	Max	Min	Max	Min	Max
1	Input Transient voltage[a]/V		V_{IS}	T_A=25℃，小于 100ms T_A=25℃，less 100ms	-	50	-	50	-	50
2	Input under-voltage	turn-on voltage	$V_{INL-ONT}$		-	17.9	-	17.9	-	17.9
		Turn-off voltage	$V_{INL-OFF}$		14.8	-	14.8	-	14.8	-
3	Input over turn-off/on voltage		$V_{INL-ON/OFF}$		36.3	39.6	36.3	39.6	36.3	39.6
4	Inhibitedinput current/mA		I_{INH}	T_A=25℃	-	15.0	-	15.0	-	15.0
5	**B**ias voltage for PC port/V		V_{PC}	T_A=25℃，I_{PC}=1.0mA	5.50	6.50	5.50	6.50	5.50	6.50
6	Current for PC port[a]/mA		I_{PC}	T_A=25℃，V_{PC}=5.5V	1.5	3.0	1.5	3.0	1.5	3.0
7	Inhibitedfunction for PC port/mV		V_{INH-PC}	T_A=25℃	2.3	2.9	2.3	2.9	2.3	2.9
8	Turn-on delay for PC port		$T_{d（ON）}$	T_A=25℃	-	7	-	7	-	7
9	alarm voltage for PC port[a]/V	peak/V	V_{A-PC}	T_A=25℃ Alarm will be turn on when input under-voltage or input over voltage	-	6.5	—	6.5	—	6.5
		period/ms	T_{PC}		1	10	1	10	1	10
		pulse/μs	W_{PC}		350	450	350	450	350	450

10	Resistance for PC port[a]/MΩ	R_{I-PC}	T_A=25℃		0.9	1.1	0.9	1.1	0.9	1.1
11	Output voltage amplitude for PR/V	V_{out-PR}	T_A=25℃，PR load over 30Ω,capacitance less 30pF		5.7	6.1	5.7	6.1	5.7	6.1
12	Output current for PR port	I_{out-PR}	T_A=25℃		150	-	150	-	150	-
13	Impedance for PR port input[a]/Ω	Z_{I-PR}	T_A=25℃		375	625	375	625	375	625
14	Input voltage threshold vale for PR port[a]/V	V_{I-PR}	T_A=25℃，Pulse width≥20ns		2.4	2.6	2.4	2.6	2.4	2.6
15	Drive capability [a]/pc	N	T_A=25℃， no buffer amplifier circuit		-	3	-	3	-	3
16	Power distribution precision [a]/%	P_E	T_A=25℃， load≥10%		-	5	-	5	-	5
17	SC reference voltage/V	V_{b-SC}	T_A=25℃，relative negative output		1.21	1.25	1.21	1.25	1.21	1.25
18	SC alarm voltage [a]/V	V_{A-SC}	T_A=25℃，SC alarm will be turn on when input under-voltage or output over-voltage()		-	0.5	-	0.5	-	0.5
19	Induct offset voltage [a]/V	V_{SC}	T_A=25℃,each terminal＜0.25V(induction terminal is closed)		-	0.5	—	0.5	—	0.5
20	Isolation voltage(Ac RMS)/V	V_{ISO}	T_A=25℃,10s	Between input and output	3000	-	3000	-	3000	-
				Between input and baseboard	1500	-	1500	-	1500	-
				Between output and baseboard	500	-	500	-	500	-
21	Isolation resistance/MΩ	R_{ISO}	T_A=25℃，add 500V(DC)between input and output, add 500V(DC)between pin and baseboard		10	-	10	-	10	-
22	Output voltage/V	V_{out}	T_A=25℃，full-load		3.267	3.333	4.95	5.05	11.88	12.12
23	Output current/A	I_{out}			0	80	0	80	0	33.33
24	Voltage regulation/%	S_v	18 36， full-load		-	0.20	-	0.20	-	0.20
25	Load regulation/%	S_{in}	No-load full-load		-	0.20	-	0.45	-	0.20
26	Temperature coefficient/（%/℃）	Av			-	0.005	-	0.005	-	0.005
27	Output voltage regulation range/%	V_{TR}	T_A=25℃，load≥10%		10	110	10	110	10	110
28	efficiency/%	η	T_A=25℃，full-load		75.5	-	80	-	85	-
29	Ripple voltage and noise voltage (peak-peak value)/mV	V_R	BW≤20MHz， full-load		-	94	-	190	-	250

30	Output over-voltage protection point/V	Vovp	T_A=25℃	4.14	4.46	6.03	6.47	13.7	14.9
31	Static power/W	P_D	No-load	-	12	-	10.1	-	10.2
32	Output protection current/A	I_{Imax}	Output voltage decline to 95%	81.6	108	81.6	104	34	43.5
33	Short-circuit current[a]/A	I_S	T_A=25℃，V_{out}<250mV	56	108	56	104	23.3	43.5

continued table 3(b) electrical characteristics

No.	Character		Symbol	Conditions （ Unless otherwise specified ，-55℃≤T_c≤125℃，V_{IN}=28V±5%）	MV24A15M400B		MV24A24M400B		MV24A28M400B	
					Min	Max	Min	Max	Min	Max
1	Input transient voltage[a]/V		V_{IS}	T_A=25℃，less 100ms	-	50	-	50	-	50
2	Input under-voltage /V	turn-on voltage	$V_{INL-ONT}$		-	17.9	-	17.9	-	17.9
		turn-off voltage	$V_{INL-OFF}$		14.8	-	14.8	-	14.8	-
3	Input over turn-off/on		$V_{INL-ON/OFF}$		36.3	39.6	36.3	39.6	36.3	39.6
4	Inhibitedinput current/mA		I_{INH}	T_A=25℃	-	15.0	-	15.0	-	15.0
5	**B**ias voltage for PC port/V		V_{PC}	T_A=25℃，I_{PC}=1.0mA	5.50	6.50	5.50	6.50	5.50	6.50
6	Current for PC port[a]/mA		I_{PC}	T_A=25℃，V_{PC}=5.5V	1.5	3.0	1.5	3.0	1.5	3.0
7	Inhibitedfunction for PC port/mV		V_{INH-PC}	T_A=25℃	2.3	2.9	2.3	2.9	2.3	2.9
8	Turn-on delay for PC port[a]/ms		$T_{d（ON）}$	T_A=25℃	-	7	-	7	-	7
9	alarm voltage for PC port[a]/V	peak/V	V_{A-PC}	T_A=25℃ Alarm will be turn on when input under-voltage or input over voltage	-	6.5	—	6.5	—	6.5
		period/ms	T_{PC}		1	10	1	10	1	10
		pulse/μs	W_{PC}		350	450	350	450	350	450
10	Resistance for PC port[a]/MΩ		R_{I-PC}	T_A=25℃	0.9	1.1	0.9	1.1	0.9	1.1
11	Output voltage amplitude for PR/V		V_{out-PR}	T_A=25℃，PR load over 30Ω,capacitance less 30pF	5.7	6.1	5.7	6.1	5.7	6.1
12	Output current for PR port		I_{out-PR}	T_A=25℃	150	-	150	-	150	-
13	Impedance for PR port input[a]/Ω		Z_{I-PR}	T_A=25℃	375	625	375	625	375	625
14	Input voltage threshold vale for PR port[a]/V		V_{I-PR}	T_A=25℃，Pulse width≥20ns	2.4	2.6	2.4	2.6	2.4	2.6
15	Drive capability [a]/pc		N	T_A=25℃， no buffer amplifier circuit	-	3	-	3	-	3
16	Power distribution precision [a]/%		P_E	T_A=25℃， load≥10%	-	5	-	5	-	5

17	SC reference voltage/V	$V_{b\text{-}SC}$	T_A=25℃，relative negative output		1.21	1.25	1.21	1.25	1.21	1.25
18	SC alarm voltage [a]/V	$V_{A\text{-}SC}$	T_A=25℃，SC alarm will be turn on when input under-voltage or output over-voltage()		-	0.5	-	0.5	-	0.5
19	Induct offset voltage [a]/V	V_{SC}	T_A=25℃,each terminal＜0.25V(induction terminal is closed)		-	0.5	—	0.5	—	0.5
20	Isolation voltage(Ac RMS)/V	V_{ISO}	T_A=25℃,10s	Between input and output	3000	-	3000	-	3000	-
				Between input and baseboard	1500	-	1500	-	1500	-
				Between output and baseboard	500	-	500	-	500	-
21	Isolation resistance/MΩ	R_{ISO}	T_A=25℃，add 500V(DC)between input and output, add 500V(DC)between pin and baseboard		10	-	10	-	10	-
22	Output voltage	V_{out}	T_A=25℃，full-load		14.85	15.15	23.76	24.24	27.72	28.28
23	Output current	I_{out}			0	26.67	0	16.67	0	14.29
24	Voltage regulation/%	S_v	18 36， full-load		-	0.20	-	0.20	-	0.20
25	Load regulation/%	S_{in}	No-load full-load		-	0.40	-	0.20	-	0.20
26	Temperature coefficient/（%/℃）	Av			-	0.005	-	0.005	-	0.005
27	Output voltage regulation range/%	V_{TR}	T_A=25℃，load≥10%		10	110	10	110	10	110
28	efficiency/%	η	T_A=25℃，full-load		86.1	-	87	-	86	-
29	Ripple voltage and noise voltage (peak-peak value)/mV	V_R	BW≤20MHz， full-load		-	75	-	100	-	215
30	Output over-voltage protection point/V	Vovp	T_A=25℃		17.1	18.5	27.1	29.1	31.5	33.9
31	Static power/W	P_D	No-load		-	9.4	-	12	-	9.5
32	Output protection current/A	I_{Imax}	Output voltage decline to 95%		27.2	34.8	17.0	21.7	14.5	19.4
33	Short-circuit current[a]/A	I_S	T_A=25℃，V_{out}<250mV		18.6	37.9	2.25	21.7	10.0	19.4

a design guarantee, test only be needed when identified inspection or parameters are effected by changing process

5 Circuit block diagram

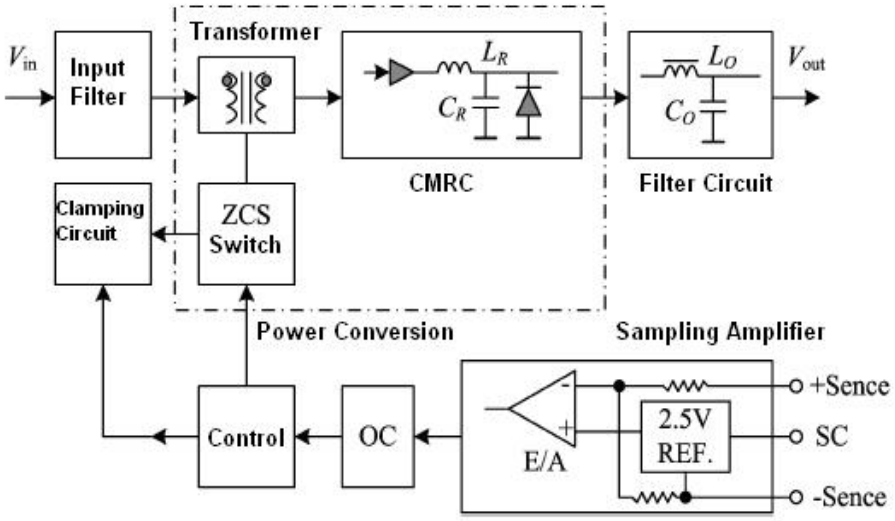


Diagram 2 Circuit block diagram

6 Typical Characteristic Curve

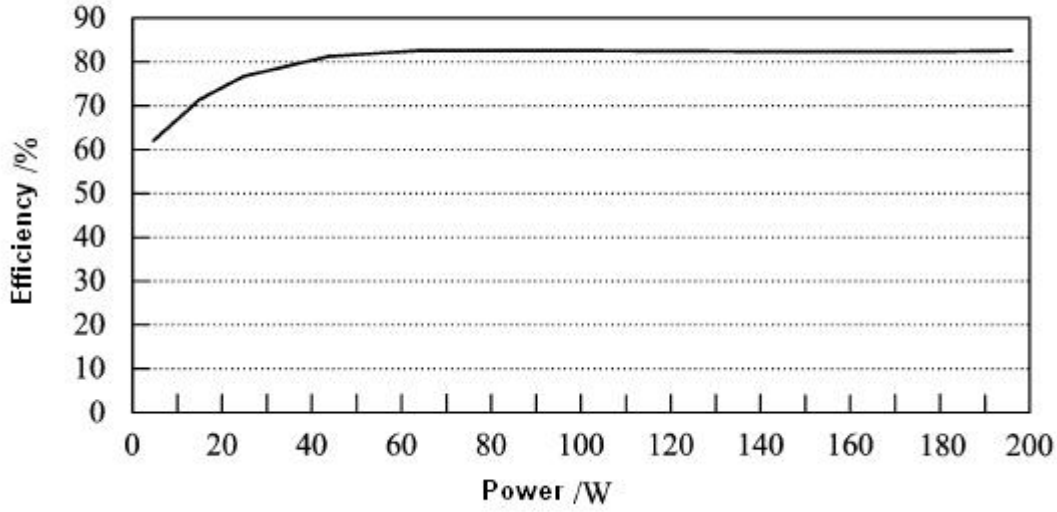


Diagram 3 Efficiency（Output power）

（MV24A5M200B model）

7 MTBF Curve

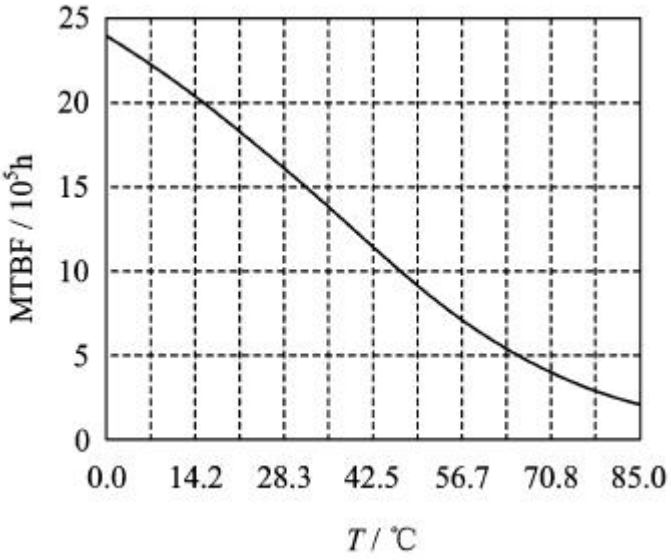


Diagram 4 MTBF Curve

(Predicting the ground is in good condition, this diagram correspond to MV24A5M400B model)

8 Pin Designation

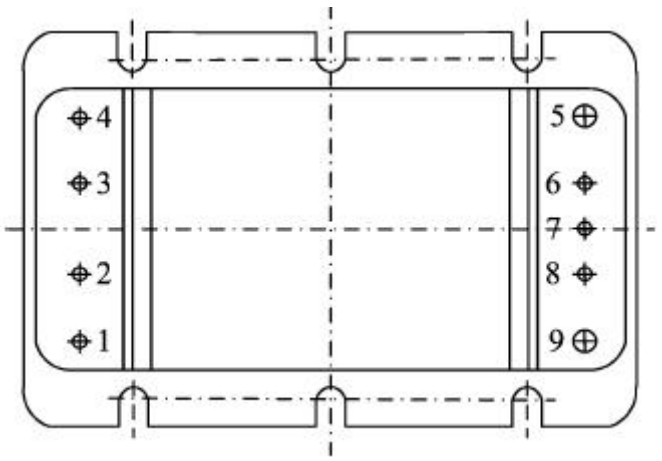


Figure 5 Pin Out Bottom View

Table 4 Pin Designation

Pin	Symbol	Designation
1	+In	Positive Input
2	PC	Prohibit/Alarm
3	PR	Parallel
4	- In	Negative Input

5	- Out	Negative Output
6	- Sence	Negative Induction
7	SC	Secondary Side Control
8	+ Sence	Positive Induction
9	+Out	Positive Output

9 Typical Connection Diagram

（1）Electrical test circuit connection diagram (diagram 6)

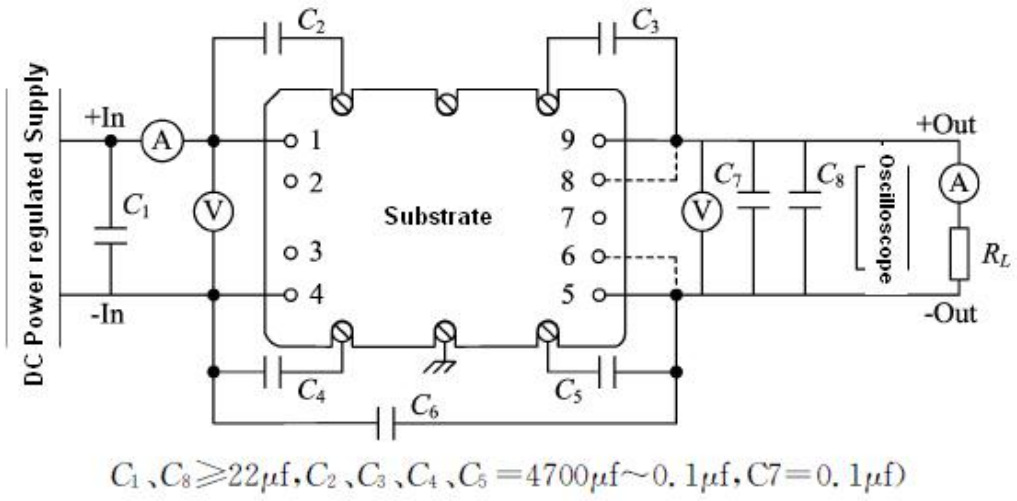
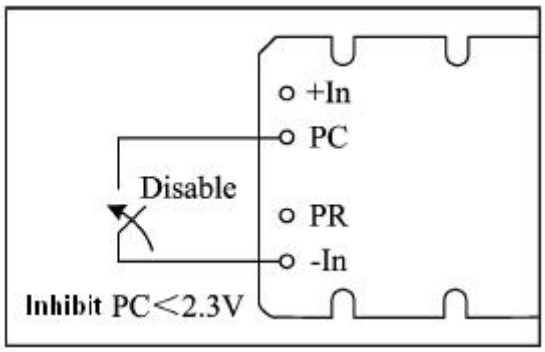


Diagram 6: Electrical test circuit connection diagram

（2）PC Prohibit and Fault Alarm （Diagram 7～9）

PC port is bi-directional port, which has module enabled function and Fault indicate function.



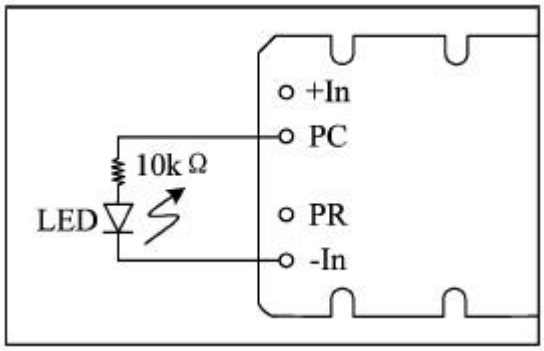


Diagram 7: module enabled

Diagram 8: Status indicate and Fault indicate

The output will be inhibited when (-In) of PC port less 2.3V, the repetition frequency of this pin should is more than 1s

LED indicator is lighted when the module is in normal operation; the indicator is flickering when over-voltage or under-voltage happened. PC port will output signal as diagram 9 when a failure happens.

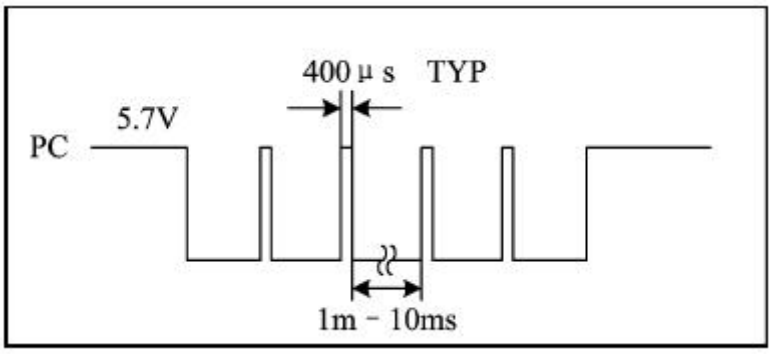


Diagram 9: Fault signal

（3）Parallel function（N+M）

Realized the paralleling and expanding current function by connected with PR ports of modules, at the same time, the fault-tolerant function is also accepted. There are two methods to realize paralleling and expanding current function, one is the automatic master-slave mode (Diagram 10) and another one is the master-slave mode (diagram 11).Under master-slave mode, the output voltage of paralleling can be adjustable by SC port of master module in accept area. Even thought both of these two methods can expand output power, the method of diagram 10 is better for system redundancy. The method of diagram 11 is better for the area in large electromagnetic interference. It must be pointed that, the cell array may be crushed by master module disabled.

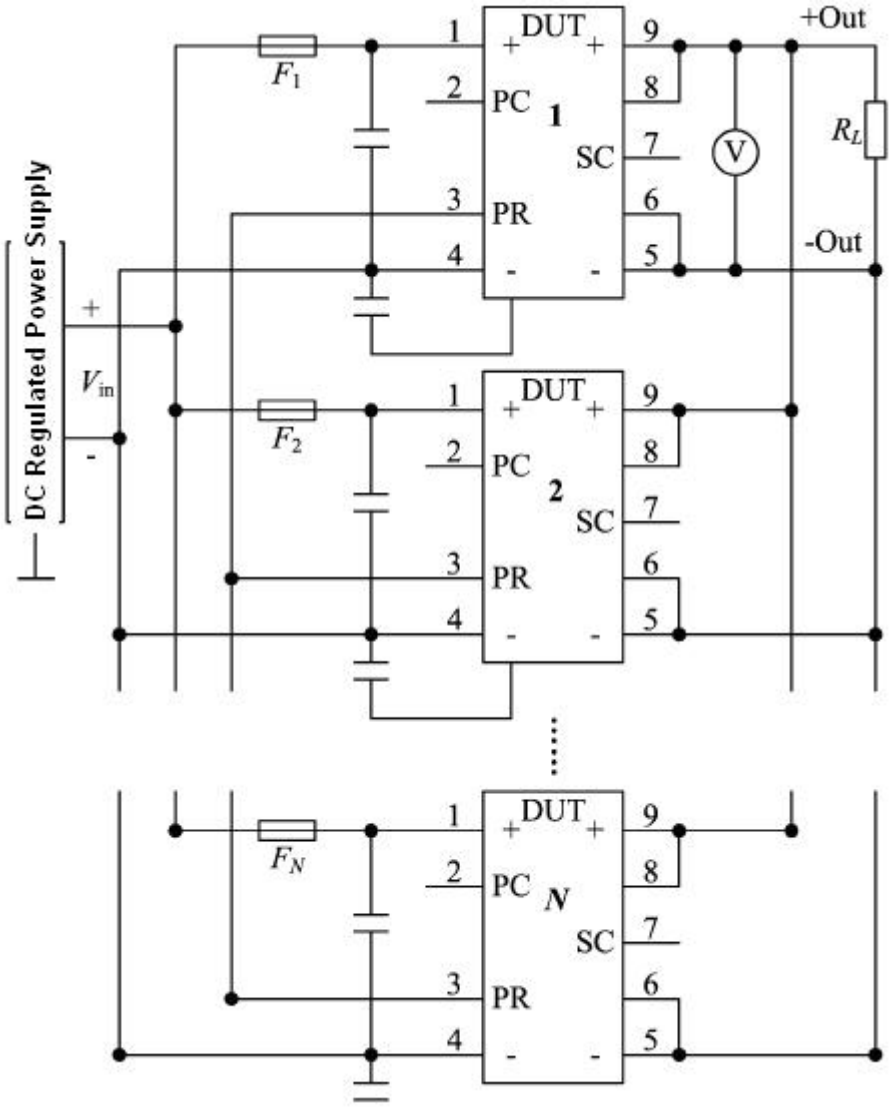


Diagram 10: Paralleling and expanding current

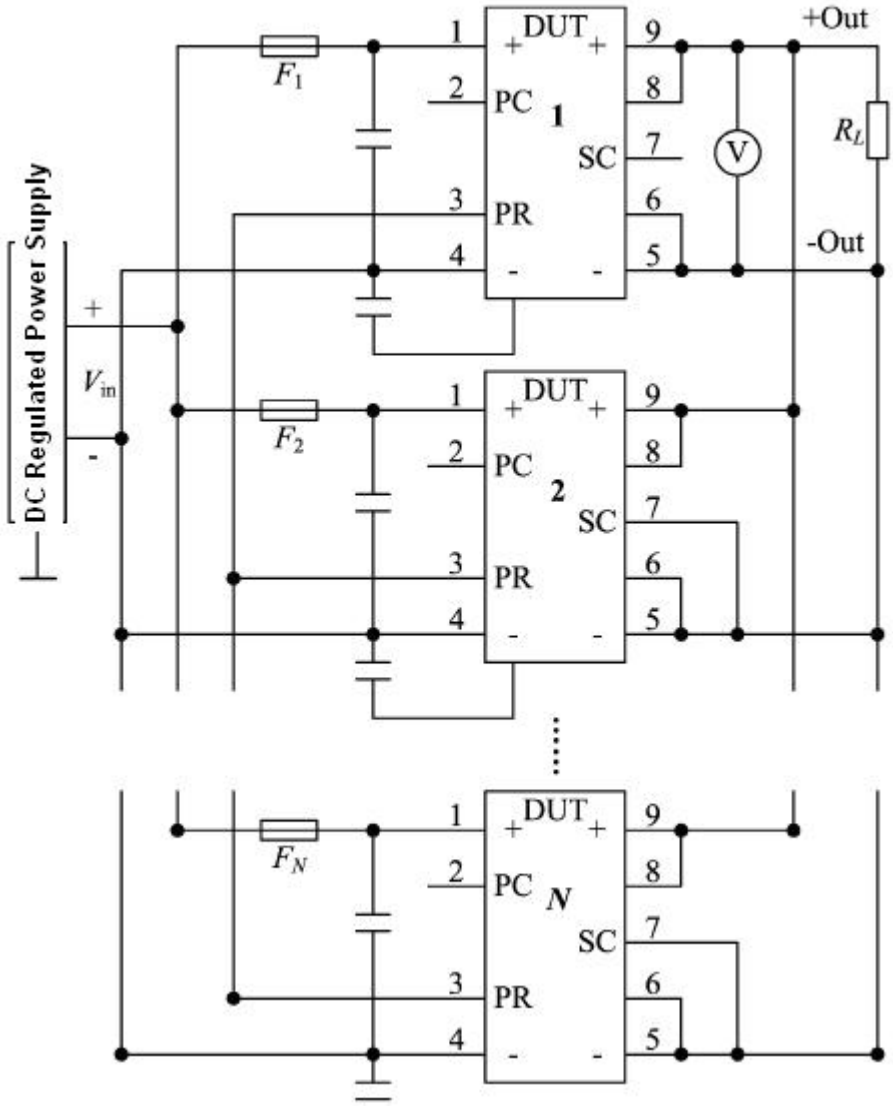


Diagram 11: Paralleling and expanding current (master-slave)

（4）Output Voltage Regulation

Connected as diagram 12, the value of output voltage and resistance RW1 are decided by the formula below

$$R_{w1} = \frac{1\,000(V_{out} - 1.23)V_{nom}}{1.23(V_{out} - V_{nom})} - 1\,000(\Omega)$$

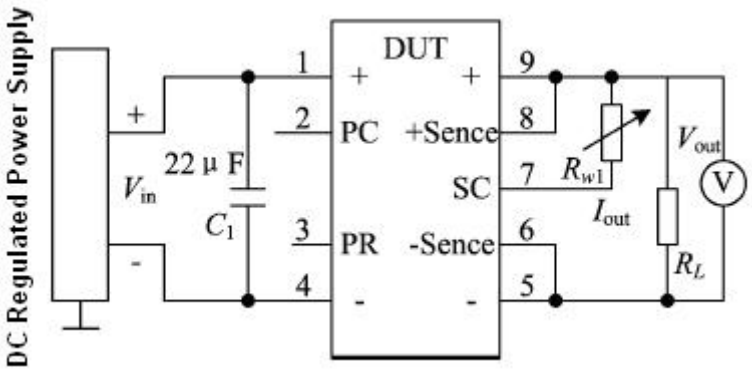


Diagram 12: Output voltage positive adjustment

Connected as diagram 13, the value of output voltage and resistance RW2 are decided by the formula below

$$R_{w2} = \frac{1\ 000V_{out}}{V_{nom} - V_{out}} (\Omega)$$

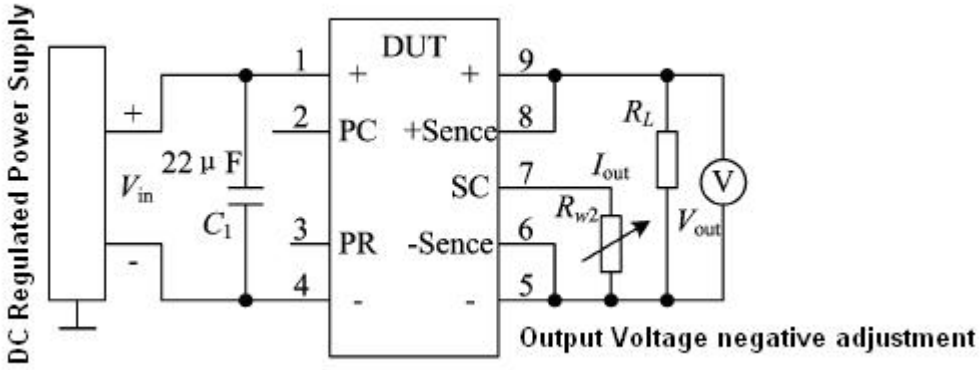


Diagram 13: Output voltage negative adjustment

10. Package Specificationss

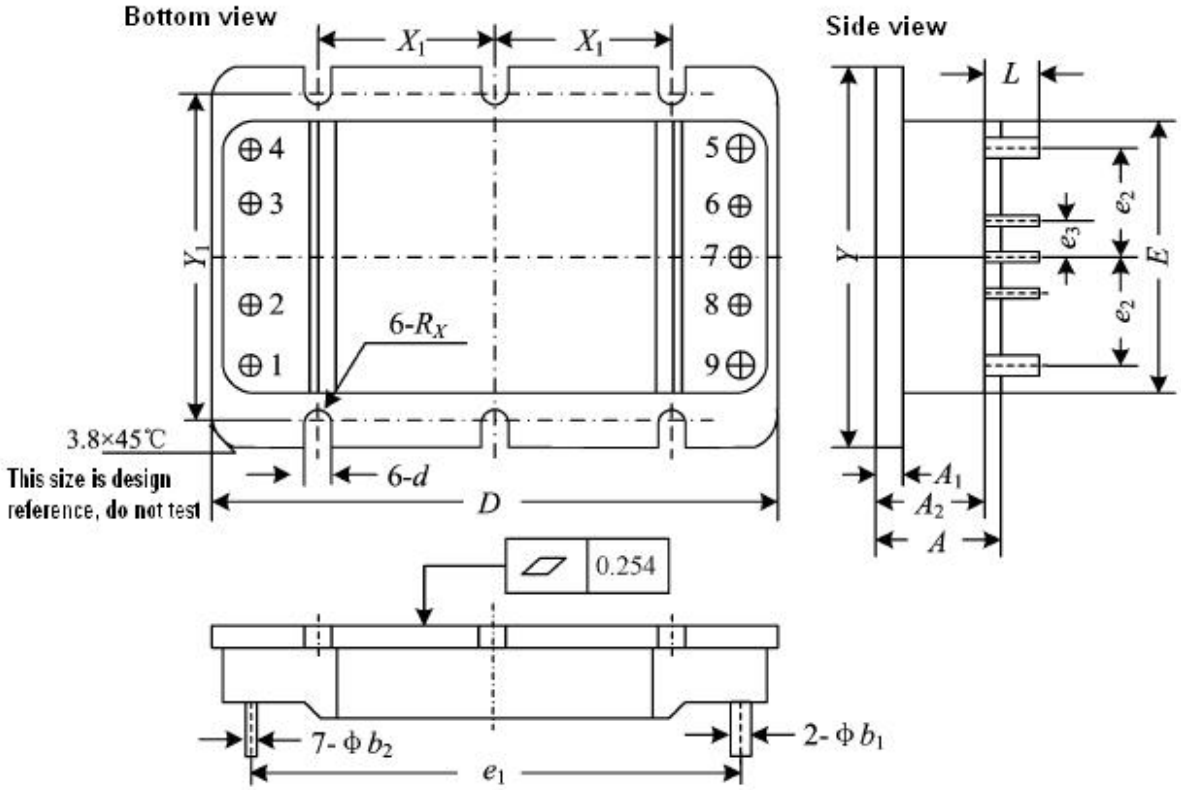


Diagram 14: Package outline drawing (upward view)

Table 5 Package Outline

Symbols	Unit/mm		
	Minimum	Typical	Maximum
A	12.20	-	13.50
A_1	2.80	-	3.30
A_2	10.65	-	11.40
Φb1	3.68	-	3.94
Φb2	1.90	-	2.16
D	116.42	-	58.28
E	43.95	-	44.95
e2	-	17.78	-
e3	-	7.62	-
e1	-	106.68	-
L	4.58	-	-
X1	45.45	-	45.95
Y1	50.55	-	51.05
d	3.17	-	3.55
Y	55.65	-	56.15

11 Ordering Information

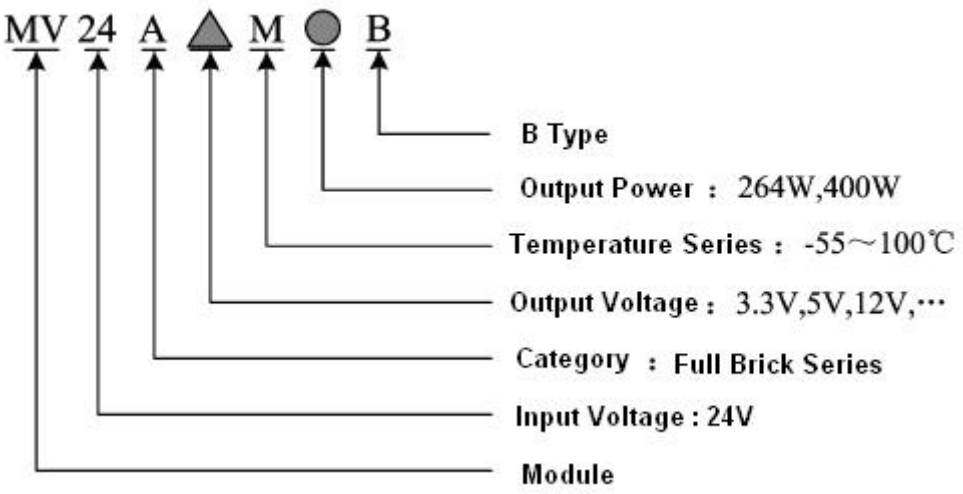


Diagram 15: Ordering Information

Application Notes:

☆ The voltage detection point should be kept at the root of the pin of the testing product.

☆ Do not plug the product with electricity.

☆ Before power the testing product, you must confirm the polarity of the power supply to avoid damaging products by misconnection. At the same time, please ensure that the power supply voltage and load current does not exceed using limitation of the testing product.

☆ Unused pins shall be hung in the air during no operation.

☆ Pins at inhibit terminal shall be hung in the air during no operation.

☆ PC and PR can not connect with +In and –In, SC can not directly connect with $+V_{out}$. Otherwise, the product may be damaged.

☆ When ordering this device，the detailed electrical specifications shall be based on relevant standards.