Synchro/Resolver-Digital Converter
(HSDC/HRDC1459 Series)

1. Features (for outside view, see Fig. 1)

Internal differential isolation conversion
16-bit resolution
Accuracy: 2 angular minutes
Three-state latch output
High continuous tracking speed
36-wire salt fog resistant metal sealed DDIP package
Pin-To-Pin compatible with Model SDC14560 of DDC company

Size: 48×20×5.3mm^3; weight: 17g
Fig.1 Outside view of HSDC/HRDC1459 Series

2. Scope of application

Military servo control system; antenna monitoring; radar control system; navigation system for naval vessels; cannon control system; flight instrument system; aviation electronic system; computerized numeric control (CNC) machine; robot technology.

3. General

HSDC/HRDC1459 series synchro/resolver-digital converter is a hybrid integrated conversion device for continuous tracking designed on the principle of model II servo. This series products are designed and manufactured by MCM process, the core elements adopt special chip developed independently by our institute. The pin arrangement is compatible with SDC14560 series products of American DDC company, 16-bit parallel natural binary code data latch output, 36-line DIP totally sealed metal package, have the advantages of high precision, small volume, low power consumption, light weight and high reliability etc., and can be widely used in important strategic and tactic weapons such as aircraft, naval vessel, cannon, missile, radar, tank, etc.

4. Electric performance (Table 1, Table 2)

Table 1 Rated conditions and recommended operating conditions

Absolute max. rated value	Logical supply voltage V_L: +7V Supply voltage Vs: ± 17.5V Signal voltage V_1: rated value ±20% Reference voltage V_{Ref}: rated value ±20% Operating frequency f: rated value ±20% Storage temperature T_{stg}: -65~150℃
Recommended operating conditions	Logical supply voltage V_L: 5±0.5V Supply voltage Vs: 15± 0.75V Signal voltage V_1: rated value ±10% Reference voltage V_{Ref}: rated value ±20% Operating frequency f: rated value ±20% Range of operating temperature (T_A): -55℃~125℃

Note: * indicates it can be customized as per user's requirement.

Table 2 Electric characteristics

Parameter	Conditions	HSDC14569 Series	
	(V_S=15V, V_L=+5V)	Military standard (Q/HW20725-2006)	
		Min.	Max.
Resolution	Binary system parallel digital code	16 bits	—
Accuracy	± 10% of signal voltage, reference voltage and fluctuation range of operating frequency	-2 angular minutes	+2 angular minutes
Range of reference frequency	—	50Hz	2600Hz
Range of reference	—	2V	115V

voltage			
Reference input impedance	—	4.4kΩ	129.2 kΩ
Range of signal voltage	—	2V	90V
Signal input impedance	—	4.4kΩ	102.2 kΩ
Signal/reference phase shift	—	—70 °	+70 °
Input logic level	—	Logic “1” ≥3.3V	Logic “0” ≤0.8V
$\overline{\text{Inhibit}}$ input	—	0	0.8V
$\overline{\text{Enable}_{\text{Hi}}}$ input	—	0	0.8V
$\overline{\text{Enabale}_{\text{Lo}}}$ input	—	0	0.8V
Output logic level	—	Logic “1” ≥3.3V	Logic “0” ≤0.8V
Digital angle code output	—	Logic “1” ≥3.3V	Logic “0” ≤0.8V
Converting busy signal (CB) output	—	200ns	600ns
Fault detection Bit output	—	Logic “0” indicates fault	
Loading capacity	—	—	3TTL
Tracking speed	—	—	2.5rps
Acceleration constant	—	—	12500
Settling time	—	—	850ms
Angular velocity voltage (Vel) output	—	—10V	+10V
Current	V_S=+15V V_S =—15V V_L=+15V	—	10mA 15 mA 20 mA

5. Step response

When a step or initial power-on happens in the input signal, the response will be inhibited due to the limitation of maximum tracking speed. The oscillation process of the output digital angle is shown in Fig. 2:

6. Operating principle (Fig. 3)

The input signal of synchro (or resolver) is converted into the orthogonal signal through the internal differential isolation:

$$Vsin=KE_0 sin(\omega t+\alpha)\sin\theta \quad (sin)$$

$$Vcos=KE_0 sin(\omega t+\alpha)\cos\theta \quad (cos)$$

Where, θ is the analog input angle.

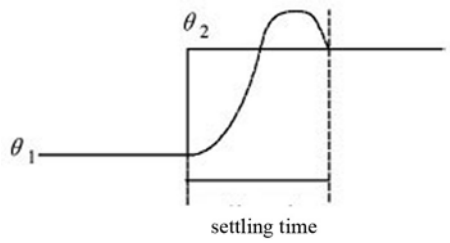

Fig.2 Curve of step response

These two signals and the digital angle φ of internal reversible counter are multiplied in the multiplier of Sine and Cosine functions and are error treated:

$KE_0 sin(\omega t+\alpha)(\sin\theta\cos\square-\cos\theta\sin\square)$, i.e. $KE_0 sin(\omega t+\alpha)\sin(\theta-\square)$

The signals are sent to voltage controlled oscillator after amplification, phase discrimination and integration filtration, if θ-φ≠0, the voltage controlled oscillator will output the pulses, and the reversible counter counts, till θ-φ becomes zero within the accuracy of the converter, during this process, the conversion tracks the change of input angle all the time.

Reading method:

Following two methods are available for data transfer:

(1) $\overline{\text{Inhibit}}$ method:

After 640ns of $\overline{\text{Inable}_{\text{Lo}}}$ logic low, the output data is valid, and the converter realizes data transfer through

$\overline{\text{Enable}_{\text{Hi}}}$ and $\overline{\text{Enable}_{\text{Lo}}}$. After $\overline{\text{Inhibit}}$ is released, the system will automatically generate a pulse with width equal to the busy pulse for data updating.

(2) Bust mode:

At the rising edge of Busy pulse, the three-state reversible counter counts; at the descending edge of Busy pulse, it internally generates a latch pulse with a width equal to Busy pulse for updating the data of three-state latch, the time sequence of data transfer is shown in Fig.4, in other words, after 600ns of Busy logic low, the stable transfer of data is valid. In the asynchronous reading mode, the Busy output is CMOS-level pulse train. The width of its high and low level depends on operating frequency and rotational speed of the selected device.

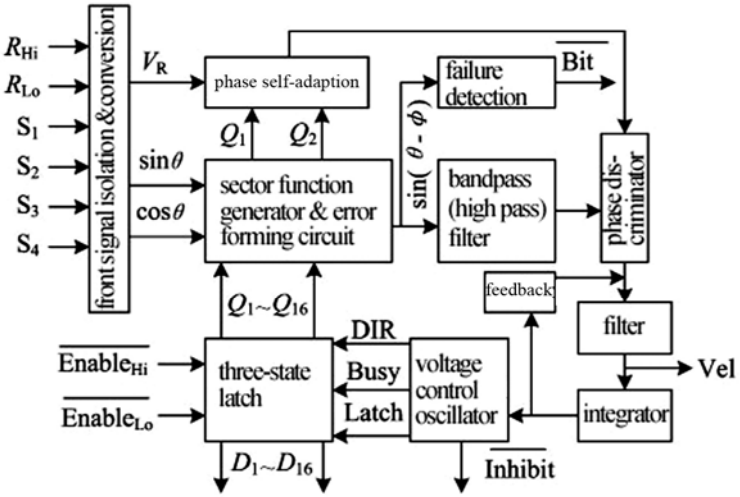

Fig. 3 Block diagram of operating principle

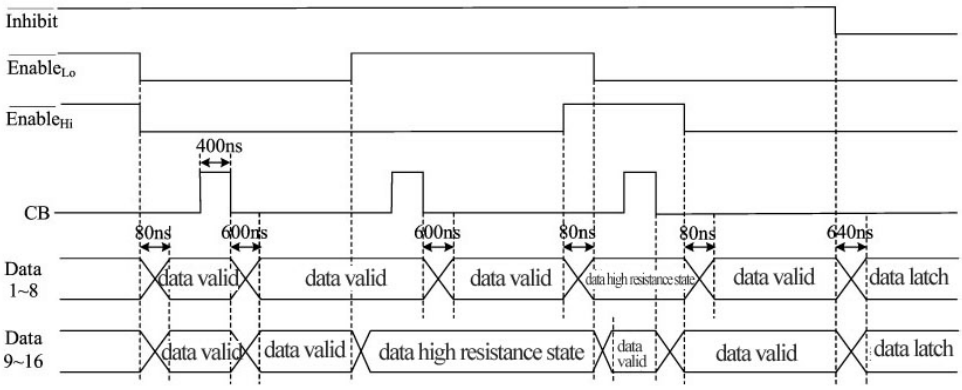

Fig.4 Time sequence of data transfer

7. MTBF curve (Fig.5)

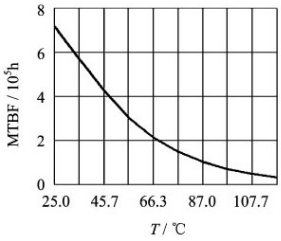

Fig.5 MTBF-temperature curve

8 Pin designation (Fig.6, Table 3)

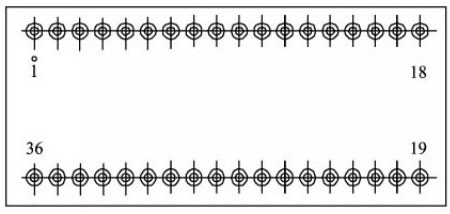

Fig.6 Pin designation (Bottom view)

(Note: according to GJB/Z299B-98, envisaged good ground condition)

Table 3 Pin designation

Pin	Symbol	Meaning	Pin	Symbol	Meaning
1	S_1	Resolver input S_1 (or synchro input S_1)	25	$\overline{Enabale_{Lo}}$	Digital Enabled control of lower 8 bits
2	S_2	Resolver input S_2 (or synchro input S_2)	26	$\overline{Enable_{Hi}}$	Digital Enabled control of higher 8 bits
3	S_3	Resolver input S_3 (or synchro input S_3)	27	RIPCLK	Zero-bit signal output
4	S_4	Resolver input S_4 (leave unconnected)	28	V_L	+5V power supply
5-18	D_1-D_{14}	Digital output 1(MSB)-14	29	GND	Ground
19	R_{Hi}	High end of reference signal input	30	NC	No connection
20	R_L	Low end of reference signal input	31	$-V_S$	-15V Power supply
21	D_{15}	Digital output 15	32	V_S	+15V Power supply
22	D_{16}	Digital output 16 (LSB)	33	$\overline{Inhibit}$	Static signal input
23	V_{el}	Angular velocity voltage signal output	34	$\overline{bit}$	Fault detection bit output
24	CB	Busy signal output	35-36	NC	No connection

Notes: D_1~D_{16} Parallel binary system digital angle code output end
S_1, S_2, S_3, S_4 Signal input of Resolver (or synchro)
R_{Hi} High end of reference signal input
R_L Low end of reference signal input

$\overline{Enabale_{Lo}}$ Lower 8-bit digit enabled signal input, this pin is the logic input pin of data gating control, its function is to carry out three-state control externally on the lower 8-bit output data of the converter. Low level is valid, the lower 8-bit output data of the converter occupies the data bus; At high level, the pin of lower 8-bit output data is in high resistance state, and the device does not occupy the data bus. Enable and release delay time is 600ns(max).

$\overline{Enable_{Hi}}$ higher 8-bit digit enabled signal input, this pin is the logic input pin of data gating control, its function is to carry out three-state control externally on the higher 8-bit output data of the converter. Low level is valid, the higher 8-bit output data of the converter occupies the data bus; At high level, the pin of higher 8-bit output data is in high resistance state, and the device does not occupy the data bus. Enable and release delay time is 600ns(max).

$\overline{Inhibit}$ static signal input, this pin is the input pin of control logic, its function is to output data externally to the converter to realize optional latching or bypass control. At high level, the output data of the converter directly outputs without latching; at low level, the output data of the converter is latched, the data is not updated, but the internal loop is not interrupted, and tracking is operating all the time, $\overline{Inhibit}$ has connected pull-up resistance internally. After 600ns (max) delay of descending edge of static signal, the data becomes stable (whether the device occupies the data bus, i.e. when does it output the data depends on the state of $\overline{Enabale_{Lo}}$ and $\overline{Enable_{Hi}}$).

CB "Busy" signal output, this signal indicates whether the binary code output of the converter is valid or not. When the change of angle input reaches 0.33 angular minute, CB end outputs a positive pulse with a width of 400ns(typical). When CB is at high level, it indicates the converter is carrying out data conversion, the data output at this time is invalid; after 600ns (max) delay of descending edge of CB signal, the data becomes stable and the updated data output at this time is valid.

$\overline{bit}$ fault detection bit output, high level indicates normal operation of the converter, in the event that the signal wire is broken or the converter fails to track normally, this bit changes into low level from high level.

RIPCLK zero-bit signal input, when the output data increment to all "0" from all "1" or decrement from all "1" from all "0", a positive pulse with a width of 200us is output.

V_L, $+V_S$, $-V_S$ Incoming terminal of power supply

GND Ground wire incoming terminal

Notes:

① Pin voltage shall not exceed 20% of rated value.

② The voltage of power supply shall not exceed the specified range.

③ Do not connect reference R_{Hi} and R_{Lo} to other pins.

④ For the power supply connected to $+V_S$ and $-V_S$ pin, its voltage shall be ±15V, and shall not be reversely connected. The digital logic power supply V_L is connected to +5V. Between the power supply and ground, 0.1μF ceramic capacitance and 6.8μF electrolytic capacitance shall be connected in parallel.

⑤ Reference signals are connected to R_{Hi} and R_{Lo}. In the case of synchro, signals are connected to S_1, S_2, and S_3 as per the following conventions.

$$E_{S_1-S_3} = E_{R_{Lo}-R_{Hi}} \sin(\omega t + \alpha) \sin\theta$$
$$E_{S_3-S_2} = E_{R_{Lo}-R_{Hi}} \sin(\omega t + \alpha) \sin(\theta + 120^\circ)$$
$$E_{S_2-S_1} = E_{R_{Lo}-R_{Hi}} \sin(\omega t + \alpha) \sin(\theta + 240^\circ)$$

⑥ In the case of resolver, signals are connected to S_1, S_2, S_3 and S_4 as per the following conventions:

$$E_{S_1-S_3} = E_{R_{Lo}-R_{Hi}} \sin(\omega t + \alpha) \sin\theta$$
$$E_{S_2-S_4} = E_{R_{Hi}-R_{Lo}} \sin(\omega t + \alpha) \cos\theta$$

Pins of CB, $\overline{\text{Inhibit}}$, $\overline{\text{Enable}_{Lo}}$, $\overline{\text{Enable}_{Hi}}$ shall all be connected as described for the above data transfer.

9 Table of weight values (Table 4)

Table 4 Table of weight values

Bit	Angle/bit	Minute/bit	Bit	Angle/bit	Minute/bit	Bit	Angle/bit	Minute/bit
1(MSB)	180.000 0	10 800	7	2.812 5	168.75	13	0.043 9	2.64
2	90.000 0	5 400	8	1.406 3	84.38	14	0.022 0	1.32
3	45.000 0	2 700	9	0.703 1	42.19	15	0.011 0	0.66
4	22.500 0	1 350	10	0.351 6	21.09	16(LSB)	0.005 5	0.33
5	11.250 0	675	11	0.175 8	10.55			
6	5.625 0	387.5	12	0.087 9	5.27			

10 Connection diagram for typical application (Fig. 7)

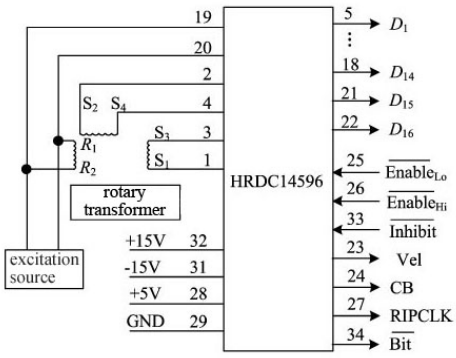

Fig. 7 Connection diagram for typical application

11 Package specifications (unit: mm) (Fig. 8, Table 5)

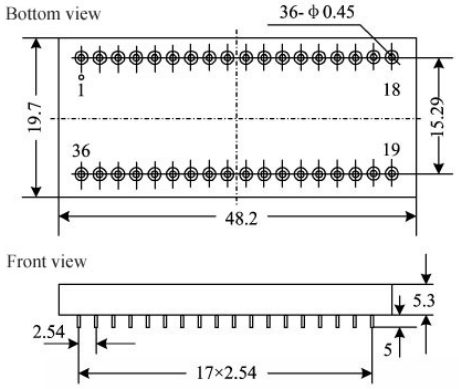

Fig.8 Outside view and dimensions of package

Table 5 Case materials

Case model	Header	Header plating	Cover	Covering plating	Pin material	Pin plating	Sealing style	Notes
UP4820-36A	4J42	Ni plating	4J42	Chemical Ni plating	4J42	Au plating	Matched seal	Header plus three solid glass beads

12 Part numbering key (Fig. 9)

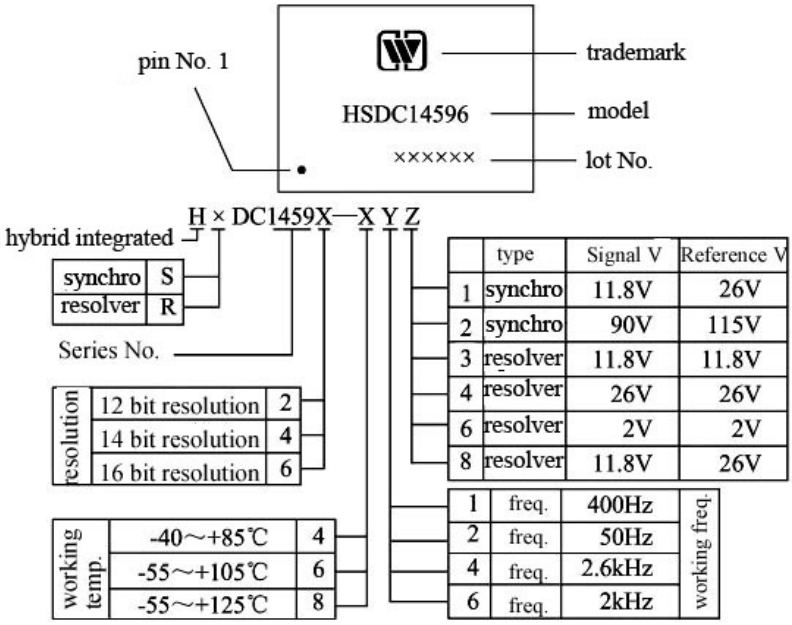

Fig.9 Part numbering key

Note: when the above signal voltage and reference voltage (Z) are non-standard, they shall be given as follows:

H ×DC 1459× — XY — ×/ ×

same as above — reference V / signal V

(e.g. reference voltage 5V and signal voltage 3V are expressed as -5/3)

Application notes:

Supply the power correctly, upon power-on, be sure to correctly connect the positive and negative pole of the power supply for fear of burnout.

Upon assembly, the bottom of the product shall fit to the circuit board closely so as to avoid damage of pins, and shockproof provision shall be added, if necessary.

Do not bend the pinouts to prevent the insulator from breaking, which affects the sealing property.

When the user places an order for the product, detailed electric performance indexes shall refer to the relevant enterprise standard.