Synchro to Digital Converter or Resolver to Digital Converter (HSDC/HRDC1746 Series)

1 Features of synchro to digital converter or resolver to digital converter (see Fig. 1 for outside view, and Table 1 for models)

- Internal differential isolation conversion
- Resolution: 16 bits
- Three-state latch output
- Uninterrupted tracking during data transfer
- 32-wire metal package

Size: 45.39×29.0×7.2mm^3
Weight: 28g
Fig. 1 Outside view of HSDC/HRDC1746 Series

Table1 Product Models

HRDC1746－418
HRDC1746－414

2 Scope of application of synchro to digital converter or resolver to digital converter

Flight instrument system; military servo control system; cannon control system; aviation electronic system; radar control system; naval vessel navigation system; antenna monitoring; robot technology, computerized numeric control (CNC) machine tools; and other automation control system.

3 Description of synchro to digital converter or resolver to digital converter

HSDC/HRDC1746 series synchro to digital converter or resolver to digital converter is designed on the principle of type II servo tracking principle and adopts differential isolation input, the data output adopts three-state latch mode, it is suitable for analog signal/digital signal conversion of three-wire synchro and four-wire resolver. With fast conversion speed and stable and reliable performance, this device can be widely applied in angle measurement and automatic control system.

This product is made by the thick-film hybrid integration process and is 32-wire DIP totally sealed metal package. Both the design and manufacture of the product satisfy the requirements of GJB2438A-2002 “General specification for hybrid integrated circuits” and specific specifications of the product.

4 Electrical performance of synchro to digital converter or resolver to digital converter (Table 2, Table 3)

Table 2 Rated conditions and recommended operating conditions

Absolute max. rated value	Supply voltage Vs: ±17.25V_{DC} Logical supply voltage V_L: +7V Storage temperature range: -55℃~150℃
Recommended operating conditions	Supply voltage Vs: ±15±5% Effective value of reference voltage V_{Ref}: ±10% of nominal value Effective value of signal voltage V^*_I: Nominal value ±5% Frequency f^* of reference signal: nominal value ±10% Phase shift between signal and excitation: ＜±10% Range of operating temperature (T_A): －40~

Table 3 Electrical characteristics

Parameter	HSDC/HRDC 1746 Series		Notes
	Min.	Max.	
Accuracy/angular minute	-2.6	2.6	
Tracking speed: rps	-3	3	
Resolution/bit	16		
Signal and reference frequency/Hz	50	2.6k	
Signal voltage (effective value)/V	2	90	
Reference voltage (effective value)/V	2	115	

	+105℃

Note: * indicates it can be customized as per user's requirement.

5 Operating principle of synchro to digital converter or resolver to digital converter

The synchro input signal (or input signal of resolver) is converted into the orthogonal signal through internal differential isolation:

$$V_1 = KE_0 \sin\theta \sin\omega t$$

$$V_2 = KE_0 \cos\theta \sin\omega t$$

Where, θ is analog input angle

The orthogonal signal is multiplied by the binary digital angle φ in the internal reversible counter in the sine-cosine function multiplier and an error function is obtained:

$$KE_0 \sin\theta\cos\varphi\sin\omega t - KE_0\cos\theta\sin\varphi\sin\omega t = KE_0 \sin(\theta-\varphi) \sin\omega t$$

Through error amplification, phase discrimination and filtration of this error function, sin(θ-φ) is obtained, when θ-φ=0 (within the accuracy of the converter), this error will make the voltage controlled oscillator output correction pulse to change the binary digital angle φ of the reversible counter so as to make the output φ value equal to the input θ within the accuracy of the converter, the system becomes stable and can track the change of input angle φ. In this way, a binary digital angle φ representing the input shaft angle θ is obtained on the reversible counter (Fig. 2).

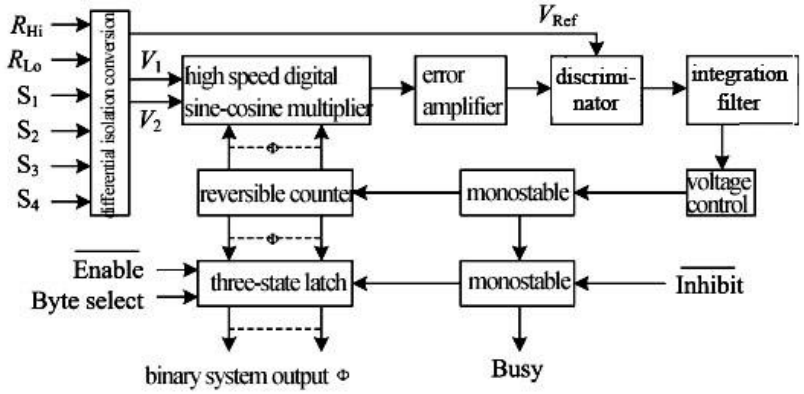


Fig. 2 Circuit block diagram

(1) Dynamic characteristics

Transfer function of the converter is shown in Fig. 3:

Open-loop gain: $\frac{\theta_{out}}{\theta_{in}} = \frac{K_a}{S^2} \bullet \frac{1+ST_1}{1+ST^2}$

Closed-loop function: $\frac{\theta_{out}}{\theta_{in}} = \frac{1+ST_1}{1+ST_1+\frac{S^2}{Ka}+\frac{S^3T_2}{Ka}}$

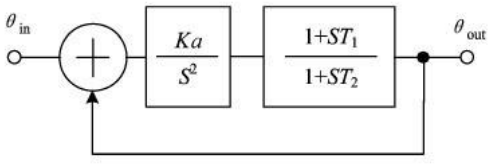


Fig. 3 Function transfer of the converter

For the module of this model Ka=48000/S², T_1=7.1ms, T_2=1.25ms

(2) Methods of data transfer and time sequence

Chip select control $\overline{\text{Enable}}$

This pin is the input pin of control logic, its function is to output data to the converter to realize three-state control. Low level is valid, the output data of converter occupies the data bus. When it is at high level, the data output pin of converter is in three states, the device does not occupy the bus.

Byte select

This pin is the control input pin, its function is to externally execute selection control on the output data of the converter in the transfer mode of 8-bit data bus or 16-bit data bus. When 16-bit data bus transfer mode is required, keep this logic pin high, the data will be transferred in the bus, the high byte output is in pin D_1 to D_8 (D_1 is high bit) and low byte is in D_9 to D_{16}. When 8-bit data bus transfer mode is needed, the data is obtained in pin D_1 to D_8 (arranged from high to low), and high 8 bits and low 8 bits are obtained through two time sequences, in other words, when Byte select is logic high, high 8 bits are output and when it is logic low, low 8 bits are output.

Data locking control (Inhibit signal $\overline{\text{Inhibit}}$)

This pin is the input pin of control logic, its function is to output data externally to the converter to realize optional latching or bypass control. At high level, the output data of the converter is directly output without latching, see the time sequence diagram of the data transfer. At low level, the output data of the converter is latched, the internal loop is not interrupted, and tracking remains working all the time, but the counter doesn't output data. When it is needed to transfer data, the converter first makes $\overline{\text{Inhibit}}$ control signal to lock the data from high to low, keeps logic low for 640ns, then set $\overline{\text{Enable}}$ input to low (at this time the device occupies the data bus), and then obtains data through Byte select, then turn all control logics to high to refresh and latch the data so as to get ready for transferring the next data, please refer to time sequence diagrams of data transfer Fig.4 and Fig.5.

(3) Attenuation method of input signal (Fig.4 and Fig.5)

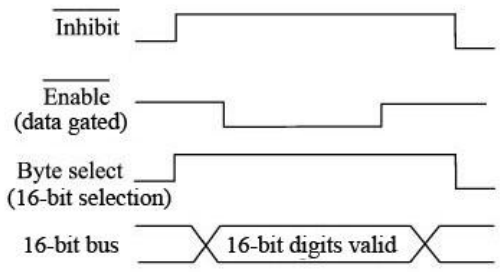


Fig4 Time sequence of 16-bit bus transfer

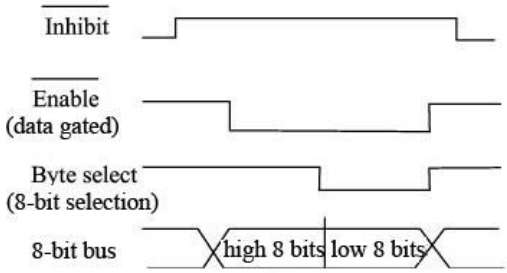


Fig5 Time sequence of 8-bit bus transfer

6 MTBF curve of synchro to digital converter or resolver to digital converter (Fig. 6)

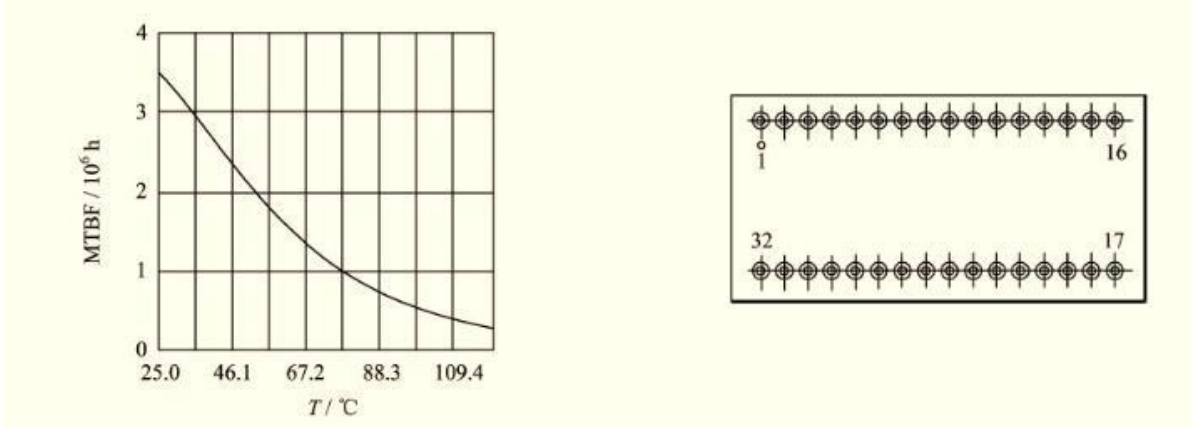


Fig.6 MTBF-temperature curve

(Note: as per GJB/Z299B-98, envisaged good ground condition)

7 Pin designation of synchro to digital converter or resolver to digital converter (Fig.7, Table 4)

Fig.7 Pin designation (Bottom view)

Table 4 Functional description of lead terminals

Pin	Symbol	Meaning	Pin	Symbol	Meaning
1	NC	No connection	17	NC	Leave unconnected
2	D_9	Digital output for 9th bit	18	R_{Hi}	Input of Resolver R_{Hi}
3	D_{10}	Digital output for 10th bit	19	R_{Lo}	Input of Resolver R_{Lo}
4	D_{11}	Digital output for 11th bit	20	GND	Ground
5	D_{12}	Digital output for 12th bit	21	$-V_S$	-15V power supply
6	D_{13}	Digital output for 13th bit	22	$+V_S$	+15V power supply
7	D_{14}	Digital output for 14th bit	23	$\overline{\text{Inhibit}}$	Control of data locking
8	D_{15}	Digital output for 15th bit	24	D_1	Digital output for 1st bit

9	D_{16}	Digital output for 16th bit	25	D_2	Digital output for 2nd bit
10	$\overline{Enable}$	Control of chip select Enable	26	D_3	Digital output for 3rd bit
11	Bysel	Byte select	27	D_4	Digital output for 4th bit
12	S_4NC①	S_4 input/no connection	28	D_5	Digital output 5th bit
13	S_3	S_3 Input	29	D_6	Digital output 6th bit
14	S_2	S_2 Input	30	D_7	Digital output 7th bit
15	S_1	S_1 Input	31	D_7	Digital output 8th bit
16	NC	No connection	32	NC	No connection

Note: ① for HSDC device, S_4 is not used.

Table 5 Table of weight values

bit (MSB)	angle	bit (MSB)	angle	bit (MSB)	angle	bit (MSB)	angle
1	180.0000	5	11.2500	9	0.7031	13	0.0439
2	90.0000	6	5.6250	10	0.3516	14	0.0220
3	45.0000	7	2.8125	11	0.1758	15	0.0110
4	22.5000	8	1.4063	12	0.0879	16	0.0055

9 Connection of the converter of synchro to digital converter or resolver to digital converter

±15V, +5V and GND shall be connected to corresponding pins on the converter, notice that the polarities of the power supply must be correct, otherwise, the converter may be damaged. It is recommended to connect 0.1μF and 6.8μF bypass capacitance in parallel between each power supply terminal and ground.

Signal and excitation source are allowed to be connected to S_1, S_2, S_3 and S_4 and R_{Hi} and R_{Lo} terminal within an error of 5%.

The signal input shall match the phase of the excitation source so that they can be correctly connected with the converter, their phases are as follows:

$$R_{Hi} \sim R_{Lo} : V_R \sin \omega t$$

For the synchro, signal inputs are:

$$For\ S_1 \sim S_3 : E_{S_1 \sim S_3} = E_{R_{L0} \sim R_{Hi}} \sin\theta \sin \omega t$$

$$For\ S_3 \sim S_2 : E_{S_3 \sim S_2} = E_{R_{L0} \sim R_{Hi}} \sin(\theta + 120°) \sin \omega t$$

$$For\ S_2 \sim S_1 : E_{S_2 \sim S_1} = E_{R_{L0} \sim R_{Hi}} \sin(\theta + 240°) \sin \omega t$$

For the resolver, signal inputs are:

$$For\ S_1 \sim S_3 : E_{S_1 \sim S_3} = E_{R_{L0} \sim R_{Hi}} \sin\theta \sin \omega t$$

$$For\ S_2 \sim S_4 : E_{S_2 \sim S_4} = E_{R_{Hi} \sim R_{Lo}} \cos\theta \sin \omega t$$

Note: no input signal of R_{Hi}, R_{Lo}, S_1, S_2, S_3 and S_4 is not allowed to be connected to other pins for fear of damage of the device.

10 Package specifications of synchro to digital converter or resolver to digital converter

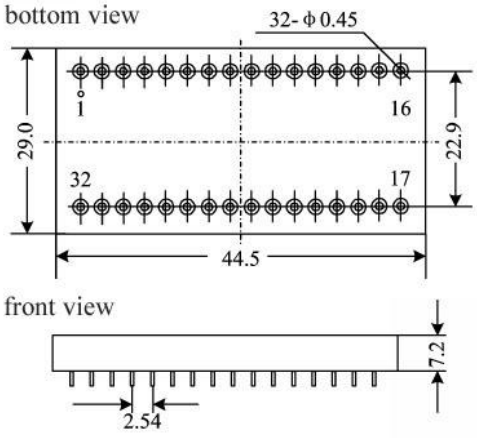


Fig.8 Outside view of package

Table 6 Case materials

Case model	Header	Header plating	Cover	Covering plating	Pin material	Pin plating	Sealing style	Notes
UP4529-32a	Kovar (4J29)	Ni	Iron/ nickel alloy (4J42)	Ni	Kovar (4J29)	Ni/Au	Matched seal	

11 Part numbering key of synchro to digital converter or resolver to digital converter (Fig. 9)

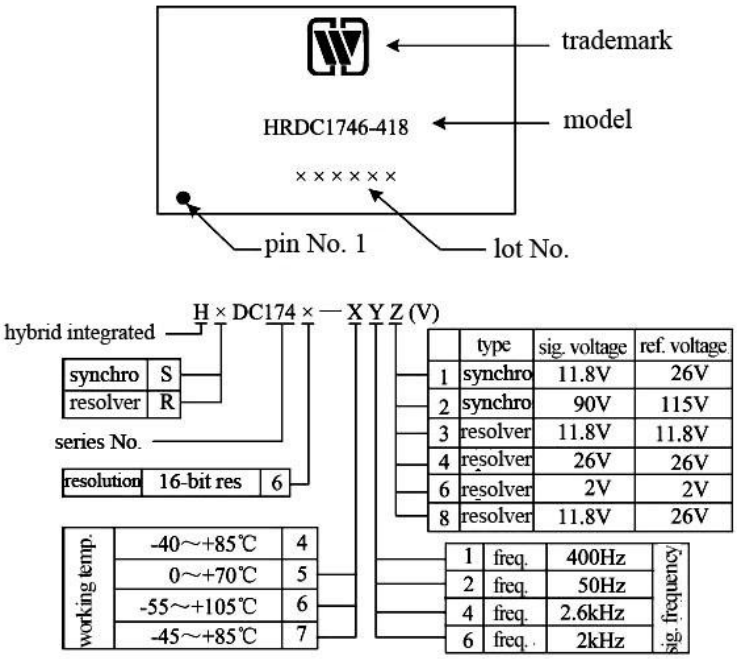
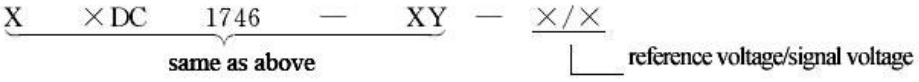


Fig.9 Part numbering key

Note: when the above signal voltage and reference voltage (Z) are non-standard, they shall be given as follows:



(e.g. reference voltage 5V and signal voltage 3V are expressed as -5/3)

Application notes of synchro to digital converter or resolver to digital converter:

- ✧ Supply the power correctly, upon power-on, be sure to correctly connect the positive and negative pole of the power supply for fear of burning.
- ✧ Upon assembly, the bottom of the product shall fit to the circuit board closely so as to avoid damage of pins, and shockproof provision shall be added, if necessary.
- ✧ Do not bend the pinouts to prevent the insulator from breaking, which affects the sealing property.
- ✧ When the user places an order for the product, detailed electric performance indexes shall refer to the relevant enterprise standard.