Two-channel Synchro to Digital Converter or Resolver to Digital Converter
(Series 2S44RDC/SDC)

1 Features of synchro to digital converter or resolver to digital converter (Outline is shown in Fig 1, Classifications are shown in Tab 1.)

- 32-wire metal case package
- Two-way independent converter, sharing the same data line
- Resolution: 14bit
- Accuracy: ±5.3′
- High tracking rate
- Pin-to-pin compatible with AD Company AD2S44 product

Size: 45×29×9.5mm³ (M2S44RDC)
45×29×7.2mm³ (H2S44RDC)
Weight: 44g(M2S44RDC)
25g(H2S44RDC)

Figure 1 Series HTS20 outline

2 Applications of synchro to digital converter or resolver to digital converter

- Antenna monitoring
- Artillery control system
- Digital servo-controlled system
- Coordinate transformation
- Platform control system

Table 1 Product classification

Synchro	Resolver
M2S44SDC-61-115/11.8	M2S44RDC-418
M2S44SDC-412	M2S44RDC-618
H2S44SDC-61-115/11.8	M2S44RDC-668
H2S44SDC-412	M2S44RDC-658
	H2S44RDC-418
	H2S44RDC-618
	H2S44RDC-668
	H2S44RDC-658

3 General description of synchro to digital converter or resolver to digital converter

Series 2S44RDC/SDC products are 14 bit two-way tracking synchro to digital converter or resolver to digital converter. They are packaged by 32-pin metal cases. They feature small sizes, light weights, high reliability and high anti-interference resistance etc.

Series 2S44RDC/SDC are two-channel converters, the two channels are independent, i.e. the two channels have independent reference voltage and input signal. Output data of 2S44RDC/SDC are connected to external data bus by 14bit output latch. The two channels are in common. The channels are selected by two control line: A/$\overline{B}$ and $\overline{OE}$.

4 Technical specifications of synchro to digital converter or resolver to digital

converter (Tab 2, Tab 3 **)**

5 Circuit theory diagram of synchro to digital converter or resolver to digital converter

Functional block diagram of series 2S44RDC/SDC is shown in figure2. Series 2S44RDC/SDC consist of two independent conversion channels. Principle of operation of each channel is the same. Principle of operation of single channel reads as follows.

Internal differential isolation converts input signals of synchro(resolver) into orthogonal signals:

$V_1=KE_0\sin\theta\sin\omega t$

$V_2=KE_0\cos\theta\sin\omega t$

Where θis analogue input angle.

The two signals are multiplied by digital angle φ of internal up/down counter in sin/cos multiplier, thus result in error signal:

$KE_0\sin\theta\cos\varphi\sin\omega t - KE_0\cos\theta\sin\varphi\sin\omega t = KE_0\sin(\theta-\varphi)\sin\omega t$

After error magnification, phase demodulator and integrator, the signal is inputted into VCO. If θ-φ≠0, VCO will output pulse, up/down counter will count untilθ-φ=0. During this process, converter continuously tracks changes of input angle.

Table2 Nominal conditions and recommended operating conditions

Absolute max nominal value	power supply voltage Vs:±17V Storage temperature range:-55~+125℃(H2S44) -40~+105℃(M2S44)
Recommended working conditions	power supply voltage Vs:±15V reference voltage(effective value)Vref:2~115V signal voltage(effective value)V_1:2~90V reference frequency f: 50Hz~10kHz operating temperature range T_A: -55~+125℃(H2S44) -40~+85℃(M2S44)

Table3 Electrical characteristics

Characteristics		Conditions	×2S44RDC/SDC Business military standard (Q/HW30826-2006) Min	Max	Units
Accuracy			-5.3	5.3	Arc min
Resolution			14	—	bit
Output	V_{outHi}		2.4	—	V
	V_{outLo}		—	0.8	
Tracking velocity			20	—	Rev/s
Repeatability			—	1	LSB
Operating frequency			2.6k	50	Hz
Band width		0°~360°	—	100	Hz
$A/\overline{B}$ and $\overline{OE}$ input	V_{IlLo}		—	0.8	V
	V_{IHi}		2.4	—	
Gate time of $A/\overline{B}$ channel	t_p		200	—	ns
Time to data stable when A/B state changes			—	640	ns
Time to data in high impedance when OE is logic "1"			—	200	ns
power dissipation			—	1.7	W

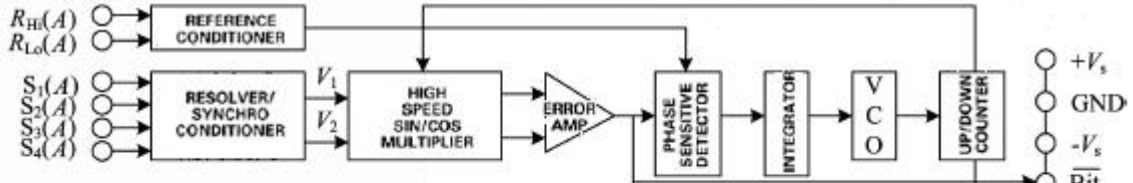


Figure2 Functional block diagram

(1) Transfer function of single channel of the converter

Open loop transfer function $\frac{\theta_{out}(S)}{\theta_{in}(S)} = \frac{Ka}{S^2} \times \frac{1+T_1S}{1+T_2S}$

Closed loop transfer function $\frac{\theta_{out}(S)}{\theta_{in}(S)} = \frac{1+T_1S}{1+ST_1+S^2/K_a+S^3T_2/Ka}$

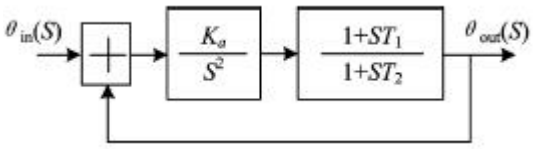


Figure3 Transfer function

(2) Channel select(A/$\overline{B}$)

A/$\overline{B}$ is the channel select input. Logic "1" selects channel A and Logic "0" selects channel B. Data become valid 640ns A/$\overline{B}$ is toggled. Timing information is shown in fig. 4.

(3) Output enable($\overline{OE}$)

$\overline{OE}$ is output enable input. When set to logic "1",D_{B1}~DB_{14} are in the high impedance state. When $\overline{OE}$ is set to logic "0",D_{B1}~DB_{14} represent the angle of transducer shaft(see bit weights in Table 5) to within the stated accuracy of the converter. Data become valid 640ns after $\overline{OE}$ is switched. Timing information is shown in fig.4.

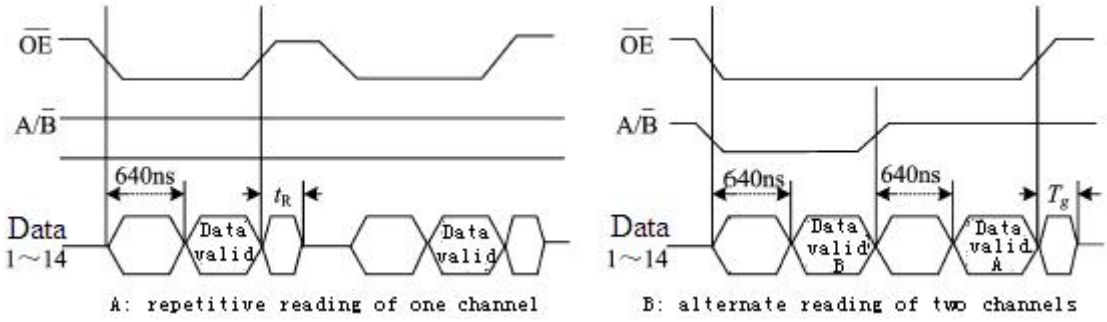


Figure 4 Timing diagrams

(4) Built-in test($\overline{BIT}$)

$\overline{BIT}$ is the built-in test error output. This provides an over velocity and fault indication signal for

the channel selected via A/$\overline{B}$. The error voltage of each channel is continuously monitored. When the error exceeds ±50bits for the currently selected channel, $\overline{BIT}$ is high level, the data are invalid. In normal condition, $\overline{BIT}$ is low level. $\overline{BIT}$ is valid for the selected channel approximately 50 ns after the change in the state of A/B.

Conditions which cause the $\overline{BIT}$ to output high level. It means the converter is in the state of no tracking.

(a) Power-up transient response
(b) Step input>1 degree
(c) Excessive velocity
(d) Signal failure
(e) Converter/system failure

6 MTBF DIAGRAM (Fig 5)

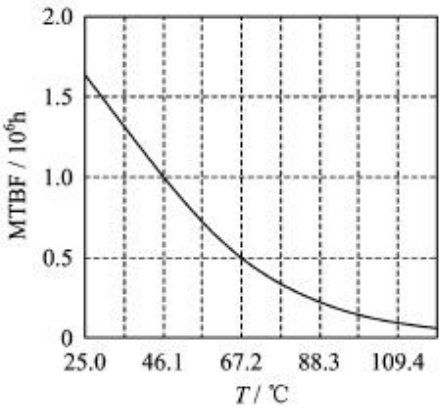


Figure 5 MTBF vs. temperature

(Note: According to GJB/Z 299B-98, assuming that ground is in good condition)

7 PIN CONFIGURATIONS (Fig6, Tab4)

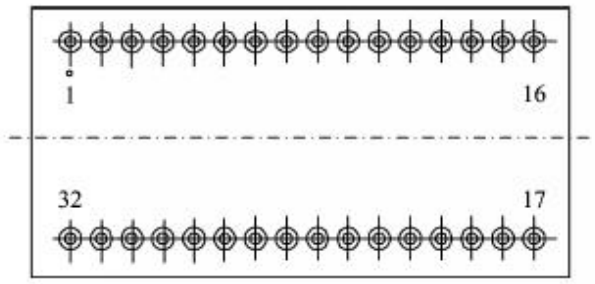


Figure 6 Pin out bottom view

Table 4 Pin description

Pin	mnemonic	description	Pin	mnemonic	description
1~7	D_8~D_{14}	Digit output	17	S_1(B)	Channel B signal input
8	$\overline{OE}$	Output enable	18	S_2(B)	Channel B signal input
9	A/$\overline{B}$	Channel selection	19	S_3(B)	Channel B signal input
10	$\overline{BIT}$	Error detection	20	S_4(B)	Channel B signal input
11	R_{Lo}(A)	Channel A reference input high pin	21	R_{Hi}(B)	Channel B reference input high pin
12	R_{Hi}(A)	Channel A reference input low pin	22	R_{Lo}(B)	Channel B reference input low pin
13	S_4(A)	Channel A signal input	23	GND	Power supply ground
14	S_3(A)	Channel A signal input	24	-Vs	-15V power supply
15	S_2(A)	Channel A signal input	25	+Vs	+15V power supply
16	S_1(A)	Channel A signal input	26~32	D_1~D_7	Digit output

8 Bit weight table of synchro to digital converter or resolver to digital converter

(Tab 5)

Table 5 Bit weight table

Bit number	Weight (degrees)	Bit number	Weight (degrees)	Bit number	Weight (degrees)
1(MSB)	180.000 0	6	5.625 0	11	0.175 8
2	90.000 0	7	2.812 5	12	0.087 9
3	45.000 0	8	1.406 3	13	0.043 9
4	22.500 0	9	0.703 1	14	0.022 0
5	11.250 0	10	0.351 6		

9 Package outline dimention and discription of synchro to digital converter or resolver to digital converter

(Unit: mm) (Fig 7,Tab 6)

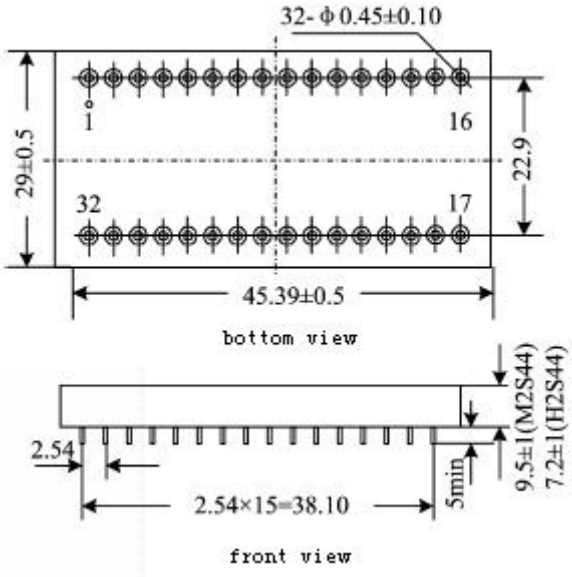


Figure 7 Package outline drawing

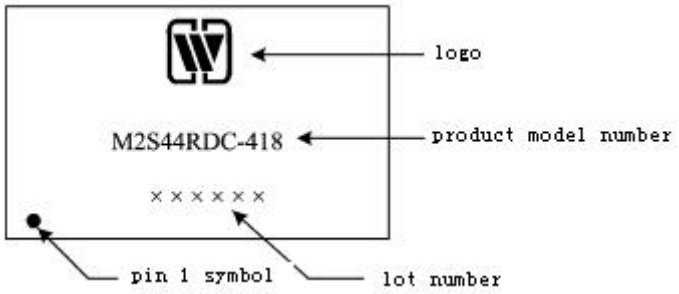
Table 6 Packaging case descriptions

Case model	Base material	Base coat	Lid(cap) material	Lid(cap) coat	Lead material	Lead coat	Sealing method	Comments
UP4429-32	Kovar	Ni	Fe/Ni	Ni	Kovar	Au	Match	

(4J29)	alloy	(4J29)	sealing

Note: The temperature of soldered pins does not surpass 300℃ within 10 sec.

10 Descriptions of product model numbering of synchro to digital converter or resolver to digital converter (Fig 8)



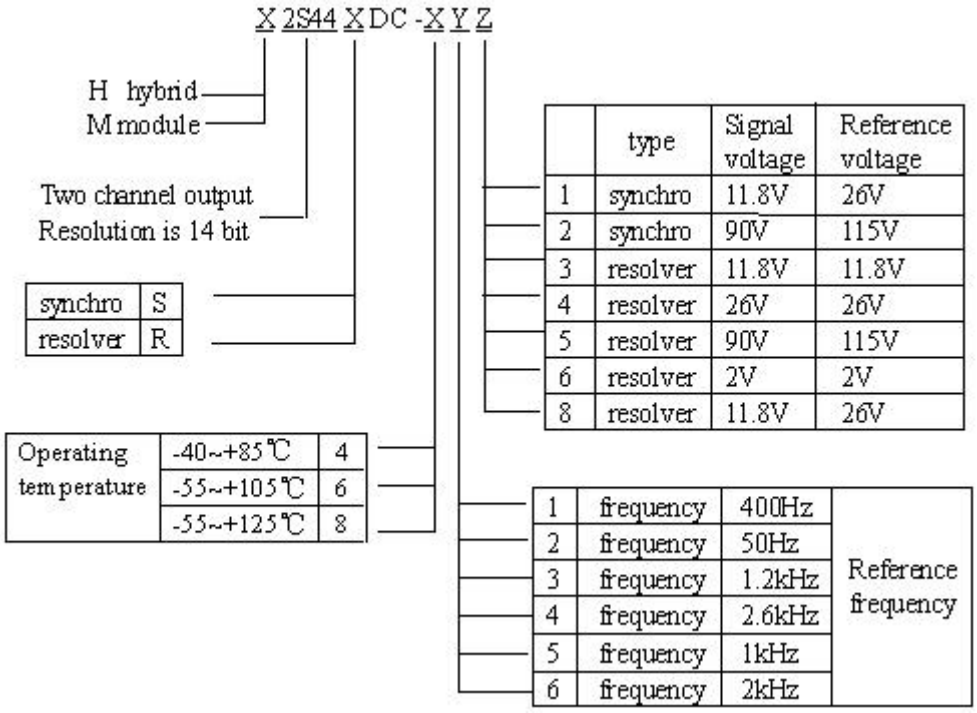


Figure8 Descriptions of product name

Note: When signal voltage and reference voltage(Z) above are not nominal, product name is given as follows:

(for example, reference voltage is 5V, signal voltage is 3V, name denotes 5/3)

Application notes of synchro to digital converter or resolver to digital converter:

★ Polar voltage of power supply should be correct.

★ When exceeding absolute maximum nominal value, it will possibly lead to damage to the device.

★ While assembling, the bottom of the product should be placed close to the board to avoid damage to the pins. If necessary, take shockproof measures.

★ Leads avoid bending, or it will easily lead to crack of insulator, which affects hermeticity.

★ When product is ordered, detailed electrical performance specifications should be referred to corresponding business standard.