Two-speed RDC Converter (Series HTS20R64)

1 FEATURES (Outline is shown in Fig 1.)

- Complete 2-speed system
- 1:64
- Digital output with 3-state latches
- Maximum resolution is 20 bit
- Maximum accuracy is 5 Arc sec

2 APPLICATIONS

- Radar
- Navigation
- Satellite tracking
- Artificial technology
- Artillery control
- Industrial machine control
- Other high-accuracy measurement

3 GENERAL DESCRI PTION

Model HTS20R64 2-speed RDC converter is single module hybrid integrated circuit packaged in metal case. They internally contain coarse/fine two way synchro/resolver-to-digital converter and error correcting logical circuit required by two speed system.

Speed ratio of coarse/fine combination of Model HTS20R64 product is1:64，speed ratio is fixed, input signals of coarse/fine two way are 4-wire resolver signals.

Size: 44×29×7.1mm^3
Weight: 30g

Figure 1 Series HTS20R64 outline

Model HTS20R64 2-speed RDC converter outputs natural parallel binary codes. Maximum is up to 20bit. They have 3-state latches.

4 TECHNICAL SPECIFICATIONS (Tab 2, Tab 3)

Table1 Nominal conditions and recommended working conditions

Absolute max nominal value	Power supply voltage Vs:±17V Storage temperature range:-65~+105℃
Recommended working conditions	Positive power supply voltage Vs:±15V Reference voltage(effective value)V_{Ref} *:26V Signal voltage(effective value)V_I*:11.8V Reference frequency f *: 400Hz Operating temperature range T_A: -55~+125℃

* means that it can be made to order.

Table2 Electrical characteristics

Characteristics	HTS20R64 Business military standard (Q/HW20905-2007)			
	Conditions V+=15±0.75V V-=-15±0.75V Signal input voltage: Vi=11.8±1.18V Exciting input voltage: V_{Ref}=26±2.6V Operating frequency: f=400±40Hz -55℃≤T_A≤125℃	**Limits**		**Units**
		Min	Max	
Resolution(RES)	0 ° ~360 °	20	-	bit
Output accuracy(r)	-	-5	5	Arc sec
Tracking velocity(S_T) Output high level(V_{outHi}) Output low level(V_{outLo})	- T_A=25℃ T_A=25℃	- 2.4 -	36 - 0.8	- V V
Power dissipation(P_D)	T_A=25℃ V+=15±0.75V V-=-15±0.75V	-	2.6	W

5 PRINCIPLES OF OPERATING (Fig 2, Fig 3)

The principles of operation for single-speed synchro-to-digital converter apply to resolver-to-digit converter.

(1) Single-peed converter

Internal differential isolation converts input signals of synchro(resolver) into orthogonal signals:

$V_1=KE_0\sin\theta\sin\omega t$, $V_2=KE_0\cos\theta\sin\omega t$

Where θ is analogue input angle.

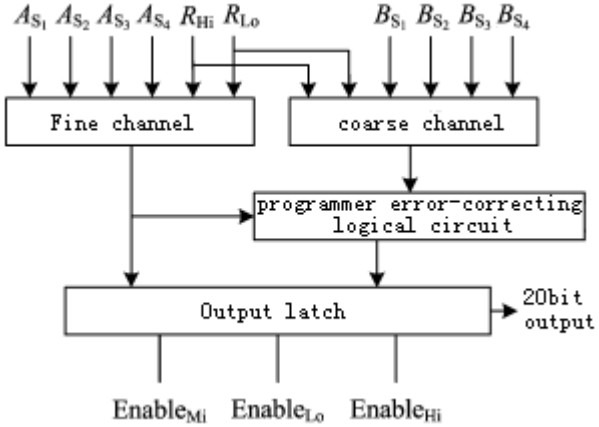


Figure2 Functional block diagram of 2-speed converter

The two signals are multiplied by digital angle φ of internal up/down counter in sin/cos multiplier, thus result in error signal:

$KE_0\sin\theta\cos\varphi\sin\omega t - KE_0\cos\theta\sin\varphi\sin\omega t=KE_0\sin(\theta-\varphi)\sin\omega t$

After error magnification, phase demodulator and integrator, the signal is inputted into VCO. If θ-φ≠0, VCO will output pulse, up/down counter will count untilθ-φ=0. During this process, converter continuously tracks changes of input angle.

(2) 2-speed converter

The principles of operation of the coarse and fine channel for the 2-speed converter are the same. Data from the coarse and fine channel first undergo data weight treatment. Then combine and correct data from fine channel and treated data from coarse channel. Finally get binary code output with 20bit resolution.

(3)Data transfer method and timing

Output of Model HTS20R64 2-speed converter reaches 20bit. Through $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ which take 3-state control of output latch, 2-speed converter can be easily connected to data bus. $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ are all valid at low level. $\overline{Enable_{Lo}}$ controls low 8bits, $\overline{Enable_{Mi}}$ controls middle 8bits, $\overline{Enable_{Hi}}$ controls rest high bits.

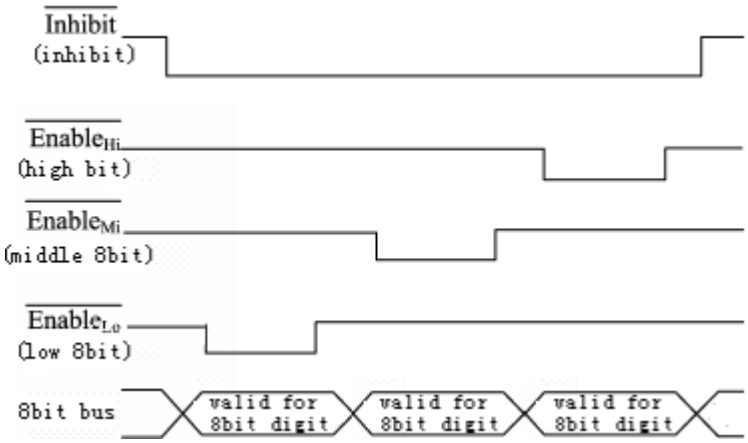


Figure 3 Timing diagrams during 8bit bus transmission

Data of Model HTS20R64 2-speed converter are rea d as follows:

Set $\overline{Inhibit}$ to logical "0", lock valid data of converter, after 1μs, data in 3-state latch of the converter are upgraded. It can read data of low 8bits, middle 8bits and high bits through controlling $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$. Figure 3 gives timing of reading data when 2-speed converter and 8 bit data bus are connected.

To ensure high-accuracy conversion of 2-speed converter, please pay attention to the following:

(1)Amplitude variation of input signals of coarse and fine channels should be guaranteed within 10% of nominal value error.

(2)Frequencies of input signals and reference signals of coarse and fine channels should be in the specified operating frequencies range.

(3)Phase shift between input signal and reference signal of coarse channel and phase shift between input signal and reference signal of fine channel should be less than 10°.

(4)Wave distortions of input signals and reference signals of coarse and fine channels should be less than 10%.

(5)Variation of +5V, ±15V power supply voltage should be guaranteed within ±5%.

6 MTBF DIAGRAM (Fig 4)

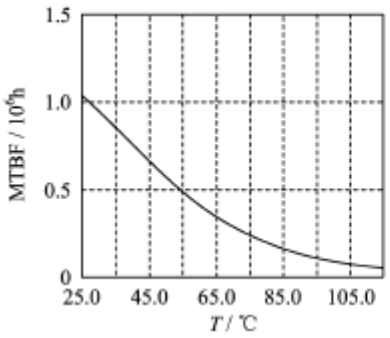


Figure 4 MTBF vs. temperature

(Note: According to GJB/Z 299B-98, assuming that ground is in good condition)

7 PIN CONFIGURATIONS (Fig5, Tab3)

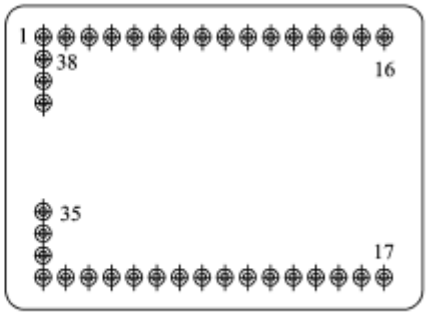


Figure 5 Pin out bottom view

Table 3 Pin description

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	$\overline{Enable_{Lo}}$	enable low 8bits control	20	DB_4	Digital output
2	$\overline{Enable_{Mi}}$	enable middle 8bits control	21	DB_5	Digital output
3	$\overline{Enable_{Hi}}$	enable high 4bits control	22	DB_6	Digital output
4	GND	ground	23	DB_7	Digital output
5	+15V	+15V input	24	DB_8	Digital output
6	-15V	-15V input	25	DB_9	Digital output
7	R_{Lo}	Input pin for reference low	26	DB_{10}	Digital output
8	R_{Hi}	Input pin for reference high	27	DB_{11}	Digital output
9	J_{S4}	Fine channel signal input	28	DB_{12}	Digital output
10	J_{S3}	Fine channel signal input	29	DB_{13}	Digital output
11	J_{S2}	Fine channel signal input	30	DB_{14}	Digital output
12	J_{S1}	Fine channel signal input	31	DB_{15}	Digital output
13	Z_{S4}	Coarse channel signal input	32	DB_{16}	Digital output
14	Z_{S3}	Coarse channel signal input	33	DB_{17}	Digital output
15	Z_{S2}	Coarse channel signal input	34	DB_{18}	Digital output
16	Z_{S1}	Coarse channel signal input	35	DB_{19}	Digital output
17	DB_1	Digital output	36	DB_{20}	Digital output
18	DB_2	Digital output	37	Busy	Busy signal output
19	DB_3	Digital output	38	$\overline{Inhibit}$	Data latch control

Note: ①connect decoupling capacitors (6.8μF/50V , 0.1μF/50V) to ±15V power supply

② $\overline{Inhibit}$ is inhibit signal, when converter is in the state of tracking, connect externally 10kΩ pull-up resistor to +5V, $\overline{Inhibit}$ is logic "1". If converter is in the state of inhibit, connect externally it to ground, $\overline{Inhibit}$ is logic "0".

③ $\overline{Enable_{Lo}}$, $\overline{Enable_{Mi}}$ and $\overline{Enable_{Hi}}$ are 3-state control pins of data output which determine state of data output. When they are logic "1", data output pin is in the state of high impedance. If they are logic "0", data output pin outputs valid data. State of data output does not affect loop operation inside converter. $\overline{Enable_{Lo}}$ controls low 8bits data, $\overline{Enable_{Mi}}$ controls middle 8bits data, $\overline{Enable_{Hi}}$ controls high 4bits data.

8 BIT WEIGHT TABLE (Tab 4)

Table 4 Bit weight table

Bit number	Weight (degrees)	Bit number	Weight (degrees)	Bit number	Weight (degrees)
1(MSB)	180.0000	8	1.1063	15	0.011(40sec)
2	90.0000	9	0.7031	16	0.0055(20sec)
3	45.0000	10	0.3516	17	0.00275(10sec)
4	22.5000	11	0.1758	18	0.00138(5sec)
5	11.2500	12	0.0879	19	6.88×10^{-4}(2.5sec)
6	5.6250	13	0.0439	20	3.44×10^{-4}(1.25sec)
7	2.8125	14	0.0220		

9 CONNECTION OF CONVERTER

±15V and ground are connected to the corresponding pins of the converter. Pay attention to the polarity of power supply, or it will harm device. It is suggested that 0.1μf and 6.8μf by-pass capacitors are connected between power supplies and ground.

Signal and exciting source are permitted to be connected to S_1,S_2,S_3,S_4 and R_{Hi} , R_{Lo} with 5% error.

Signal input should be in coordination with exciting phase, their phases are as follows:

R_{Hi} ~R_{Lo} :V_{Ref}sinωt

In the case of synchro:

S_1~S_3: $E_{S1\sim S3}=E_{RLo\sim RHi}\sin\theta\sin\omega t$

S_3~S_2: $E_{S3\sim S2}=E_{RLo\sim RHi}\sin(\theta+120°)\sin\omega t$

S_2~S_1: $E_{S2\sim S1}=E_{RLo\sim RHi}\sin(\theta+240°)\sin\omega t$

In the case of resolver:

S_1~S_3: $E_{S1\sim S3}=E_{RLo\sim RHi}\sin\theta\sin\omega t$

S_2~S_4: $E_{S2\sim S4}=E_{RHi\sim RLo}\cos\theta\sin\omega t$

Note: input signals in R_{Hi}, R_{Lo}, S_1, S_2, S_3, S_4 are not permitted to connect other pins, or it will damage the device.

Other pins should be connected according to pin definition of the device.

It is suggested that user should inform manufacturer to have device made to order according to parameters when using non-nominal synchro or resolver.

10 PACKAGE OUTLINE DIMENTION AND DISCRIPTION

(Unit: mm**) (** Fig 6, Tab 5 **)**

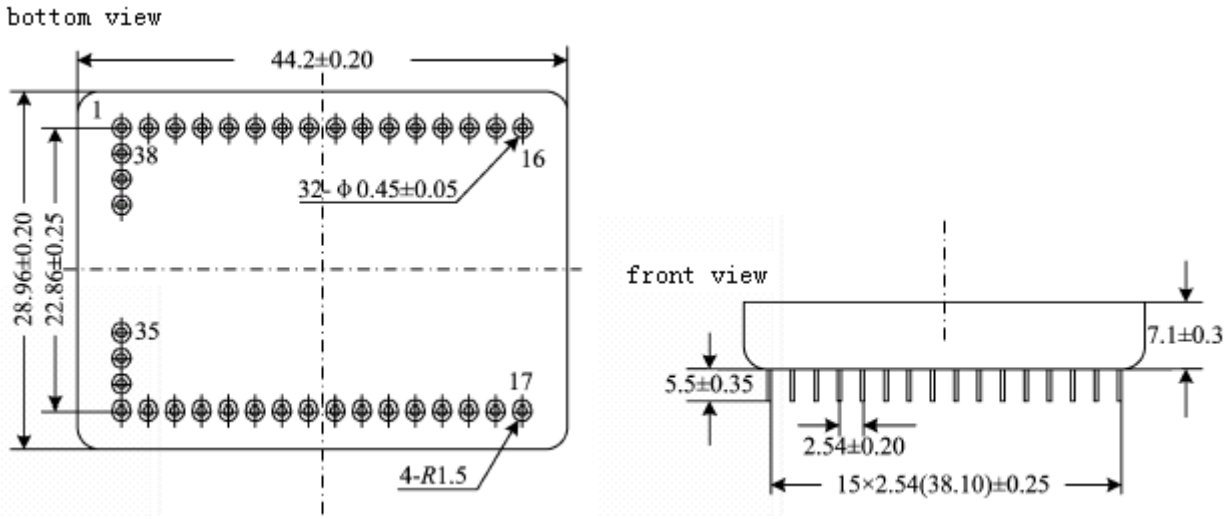


Figure 6 Package outline drawing

Table 5 Packaging case descriptions

Case model	Base material	Base coat	Lid(cap) material	Lid(cap) coat	Lead material	Lead coat	Sealing method	Comments
UP4429-28	Cold-rolled steel(10#)	Ni	Fe/Ni alloy	Ni	Au	Ni/Au	Match sealing	

Note: The temperature of soldered pins does not surpass 300℃ within 10 sec.

11 DESCRIPTIONS OF PRODUCT MODEL NUMBERING (Fig 7)

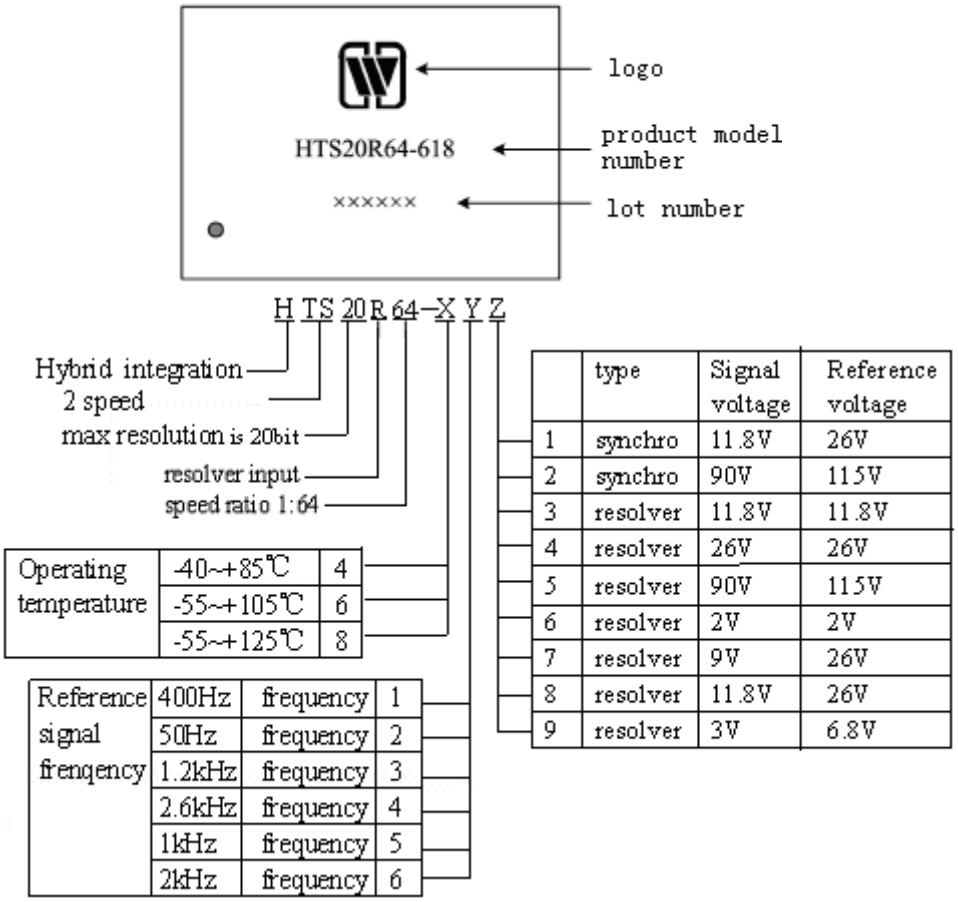
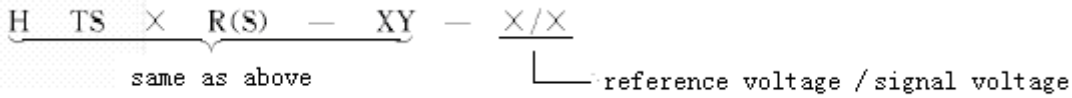


Figure 7 Descriptions of product name

Note: When signal voltage and reference voltage(Z) above are not nominal, product name is given as follows:



(for example, reference voltage is 5V, signal voltage is 3V, name denotes 5/3)

Application notes:

★Polar voltage of power supply should be correct.

★When exceeding absolute maximum nominal value, it will possibly lead to damage to the device.

★While assembling, the bottom of the product should be placed close to the board to avoid damage to the pins. If necessary, take shockproof measures.

★When product is ordered, detailed electrical performance specifications should be referred to corresponding business standard.