2-speed Miniaturized RDC/SDC Converter(Series MRDC /MSDC)

1 FEATURES (Outline is shown in Fig 1. Classifications are shown in table1)

- Complete 2-speed system
- Speed ratios are 1:8, 1:16, 1:32
- Digital output with 3-state latches
- Maximum resolution is 19 bit
- Maximum accuracy is ±10sec
- Small size

Size: 54.3×27.9×10 mm^3
Weight: 41g
Figure 1 Series MRDC/MSDC outline

Table1 Product classification

MRDC19-618(1:32)
MRDC19-61-36/11.8(1:32)
MRDC18-458(1:16)
MRDC16-66-6.8/3(1:8)
MRDC16-669(1:16)

2 APPLICATIONS

- Radar
- Navigation
- Satellite tracking
- Artificial technology
- Artillery control
- Industrial machine control
- Other high-accuracy measurement

3 GENERAL DESCRI PTION

2-speed RDC /SDC converters(series MRDC /MSDC) are monolithic circuits hermetically sealed by metal. They internally contain coarse/fine two way RDC/SDC converter and error correcting logical circuit required by two speed system.

Speed ratios of coarse/fine combination of series MRDC /MSDC product are 1:32, 1:16, 1:8, it is easy to use. Input signals of coarse/fine two way are signals of three-wire synchcro or four-wire resolver.

4 TECHNICAL SPECIFICATIONS (Tab 2, Tab 3)

Table2 Nominal conditions and recommended working conditions

Absolute max nominal value	power supply voltage +Vs:12.5~17.5V power supply voltage -Vs: -17.5~-12.5V logic voltage V_L: +7V storage temperature range:-55~+125℃
Recommended working conditions	power supply voltage Vs: ±15V±5% power supply voltage V_L: +5V±5% reference voltage(significant value)V^*_{Ref}: nominal value±10% signal voltage(significant value)V^*_I: nominal value±10% reference frequency f *: nominal value±10% operating temperature range T_A: -40~+85℃ -55~+105℃

* means that it can be made to order.

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Table3 Electrical characteristics

Characteristics	Series MRDC /MSDC	Units	Characteristics	Series MRDC /MSDC Min	Max	Units
Speed ratio	1:8 1:16 1:32		Signal voltage range (significant value)	2	90	V
Resolution	16 18 19	bit	Direction signal high level	2.4	6	V
Max accuracy	±40 ±20 ±10	Arc sec	Direction signal low level	-0.3	0.8	V
tracking velocity in fine channel①	- 16	rev/s	Inhibit input voltage	-0.3	0.8	V
frequency range	50 10000	Hz	Output high level	2.4	6	V
reference voltage (significant value)	2 115	V	Output low level	-0.3	0.8	V

① tracking velocity can be made to order.

5 PRINCIPLES OF OPERATING (Fig 2, Fig 3)

(1) Single speed converter

The principles of operation of single speed converter are shown in fig2. Principles are summarized as follows:

Internal differential isolation converts input signals of synchro(resolver) into orthogonal signals:

$V_1=KE_0\sin\theta\sin\omega t$, $V_2=KE_0\cos\theta\sin\omega t$

Where θ is analogue input angle.

The two signals are multiplied by digital angle φ of internal up/down counter in sin/cos multiplier, thus result in error signal:

$KE_0\sin\theta\cos\varphi\sin\omega t - KE_0\cos\theta\sin\varphi\sin\omega t$

$=KE_0\sin(\theta-\varphi)\sin\omega t$

After error magnification, phase demodulator and integrator, the signal is inputted into VCO. If θ-φ≠0, VCO will output pulse, up/down counter will count untilθ-φ=0. During this process, converter continuously tracks changes of input angle.

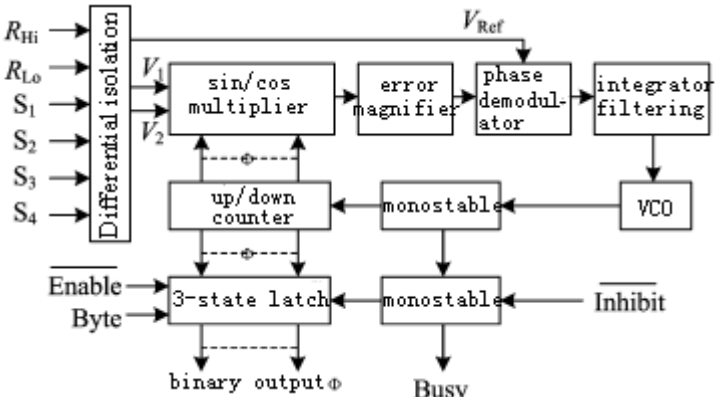

Figure2 Functional block diagram of single speed converter

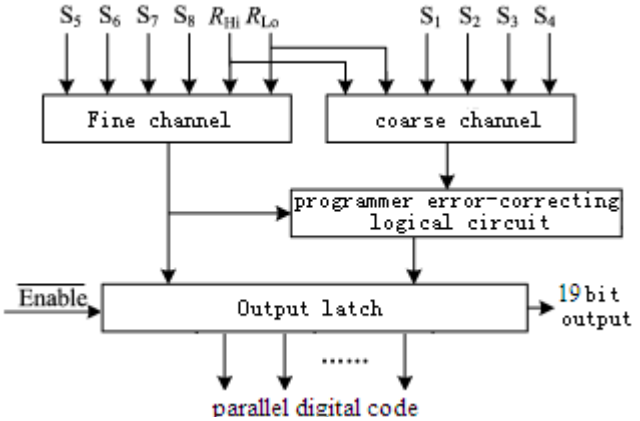

Figure3 Functional block diagram of 2 -speed converter

(2) 2-speed converter

The principles of operation for single-speed RDC/SDC converter apply to 2-speed RDC/SDC converter. The principles of operation of the coarse and fine channel for the 2-speed converter are the same. Data from the coarse and fine channel first undergo data weight treatment, i.e. increase multiple of data speed ratio in coarse channel. Then combine and correct data from fine channel and treated data from coarse channel. Finally get binary code output(fig.3).

(3) Data transfer method and timing

Output of MDRC19 2-speed converter reaches 19bit. Through $\overline{\text{Enable}}$ which take 3-state control of output latch, 2-speed converter can be easily connected to data bus.

Data of MDRC19 2-speed converter are read as follows:

Set $\overline{Inhibit}$ to logical "0", lock valid data of converter, after 1μs, data in 3-state latch of the converter are upgraded.

To ensure high-accuracy conversion of 2-speed converter, please pay attention to the following:

① Amplitude variation of input signals of coarse and fine channels should be guaranteed within 10% of nominal value error.

② Frequencies of input signals and reference signals of coarse and fine channels should be in the specified operating frequencies range.

③ Phase shift between input signal and reference signal of coarse channel and phase shift between input signal and reference signal of fine channel should be less than 10°.

④ Wave distortions of input signals and reference signals of coarse and fine channels should be less than 10%.

⑤ Variation of +5V, ±15V power supply voltage should be guaranteed within ±5%.

6 MTBF DIAGRAM (Fig 4)

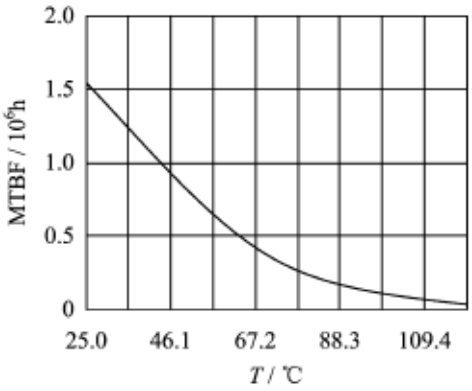

Figure 4 MTBF vs. temperature

(Note: According to GJB/Z 299B-98, assuming that ground is in good condition)

7 PIN CONFIGURATIONS (Fig 5, Tab 4)

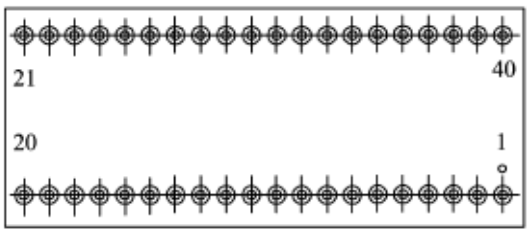

Figure 5 Pin out bottom view

Table 4 Pin description

Pin	mnemonic	description	Pin	mnemonic	description
1	D_1(MSB)	Data output 1st bit	21	S_8	Fine channel cos signal input
2	D_2	Data output 2nd bit	22	S_7	Fine channel sin signal input
3	D_3	Data output 3rd bit	23	S_6	Fine channel cos signal input
4	D_4	Data output 4th bit	24	S_5	Fine channel sin signal input
5	D_5	Data output 5th bit	25	R_{Lo}	Reference input low
6	D_6	Data output 6th bit	26	R_{Hi}	Reference input high
7	D_7	Data output 7th bit	27	S_4	Coarse channel cos signal input
8	D_8	Data output 8th bit	28	S_3	Coarse channel sin signal input
9	D_9	Data output 9th bit	29	S_2	Coarse channel cos signal input
10	D_{10}	Data output 10th bit	30	S_1	Coarse channel sin signal input
11	D_{11}	Data output 11th bit	31	NC	Not connected
12	D_{12}	Data output 12th bit	32	case	Case ground
13	D_{13}	Data output 13th bit	33	DIR	Direction signal output pin
14	D_{14}	Data output 14th bit	34	$\overline{\text{Enable}}$	Output control pin
15	D_{15}	Data output 15th bit	35	$\overline{Inhibit}$	Inhibit input pin
16	D_{16}	Data output 16th bit	36	busy	Busy signal output pin
17	D_{17}	Data output 17th bit	37	+Vs	+15V power supply input pin
18	D_{18}	Data output 18th bit	38	GND	ground
19	D_{19}(LSB)	Data output 19th bit	39	-Vs	-15V power supply input pin
20	Vel	Velocity output signal pin	40	V_L	+5V power supply input pin

Note: ① S_8,S_7, S_6,S_5 are fine channel input. If synchro is equipped with three wire, S_8 is not used.

② S_4,S_3, S_2,S_1 are coarse channel input. If synchro is equipped with three wire, S_4 is not used.

③ $\overline{Inhibit}$ is inhibit signal which is connected to 5V power supply by pull-up resistor. When $\overline{Inhibit}$ is logical "0", After 1μs, data in latch are stable, data can be read. When $\overline{Inhibit}$ is logical "1", data in latch upgrade. $\overline{Inhibit}$ does not affect the tracking state of loop.

④ $\overline{\text{Enable}}$ are three state control pins of data output, which determined the state of outputted data. When they are logical "1", data output pin is in high impedance. When they are logical "0", data output pin outputs valid data. Outputted data state doesn't affect the loop operation inside converter.

⑤ DIR is direction signal input pin. When outputted digits increase, output voltage is in high level. When outputted digits decrease, output voltage is in low level.

⑥ Vel is velocity output signal. This signal can be drawn from fine channel. It also can be drawn from coarse channel according to customer's requirement.

⑦ D_1~D_{20} are Outputs of combined digital angle. D_1 is most significant bit. D_{20} is least significant bit. D_{17}~D_{19} is not used.

8 BIT WEIGHT TABLE (Tab 5)

Table 5 Bit weight table

Bit No. (MSB)	Weight (degrees)	Bit No. (MSB)	Weight (degrees)	Bit No. (MSB)	Weight (degrees)
1	180.000 0	8	1.106 3	15	0.011 0
2	90.000 0	9	0.703 1	16(LSB 16 bit)	0.005 5
3	45.000 0	10	0.351 6	17	0.00275
4	22.500 0	11	0.175 8	18(LSB 18 bit)	0.001 375
5	11.250 0	12	0.087 9	19(LSB 19 bit)	0.000 687 5
6	5.625 0	13	0.043 9		
7	2.812 5	14	0.022 0		

9 TYPICAL CONNECTION OF CONVERTER (Fig 6)

±15V, 5V and ground are connected to the corresponding pins of the converter. Pay attention to the polarity of power supply, or it will harm device. It is suggested that 0.1μf and 6.8μf by-pass capacitors are connected between power supplies and ground.

Signal and exciting source are permitted to be connected to S_1,S_2,S_3,S_4 and R_{Hi} , R_{Lo} with 5% error.

Signal input should be in coordination with exciting phase, their phases are as follows:

R_{Hi} ~R_{Lo} :V_{Ref}sinωt

In the case of synchro:

S_1~S_3: $E_{S1\sim S3}=E_{RLo\sim RHi}\sin\theta\sin\omega t$

S_3~S_2: $E_{S3\sim S2}=E_{RLo\sim RHi}\sin(\theta+120°)\sin\omega t$

S_2~S_1: $E_{S2\sim S1}=E_{RLo\sim RHi}\sin(\theta+240°)\sin\omega t$

In the case of resolver:

S_1~S_3: $E_{S1\sim S3}=E_{RLo\sim RHi}\sin\theta\sin\omega t$

S_2~S_4: $E_{S2\sim S4}=E_{RHi\sim RLo}\cos\theta\sin\omega t$

Note: input signals in R_{Hi}, R_{Lo}, S_1, S_2, S_3, S_4 are not permitted to connect other pins, or it will damage the device.

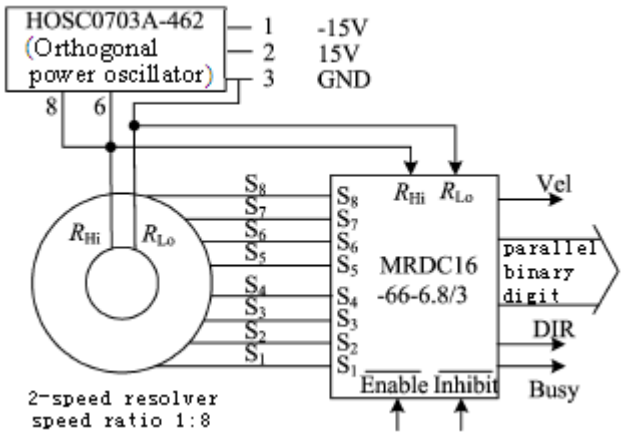

Figure6 Typical connection

10 PACKAGE OUTLINE DIMENTION AND DISCRIPTION

(Unit: mm) (Fig 7, Tab 6)

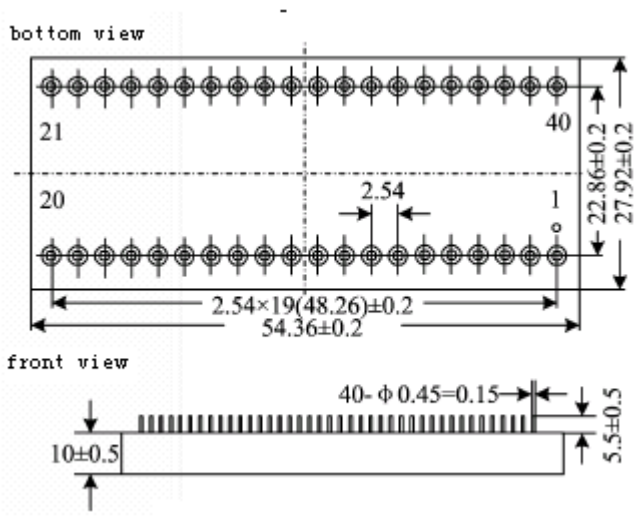

Figure 7 Package outline drawing

Table 6 Packaging case descriptions

Case model	Base material	Base coat	Lid(cap) material	Lid(cap) coat	Lead material	Lead coat	Sealing method	Comments
UP5428-40	Kovar (4J29)	Ni/Au	Fe/Ni alloy	Ni/Au	Kovar (4J29)	Ni/Au	Match sealing	

Note: The temperature of soldered pins does not surpass 300℃ within 10 sec.

11 DESCRIPTIONS OF PRODUCT MODEL NUMBERING (Fig 8)

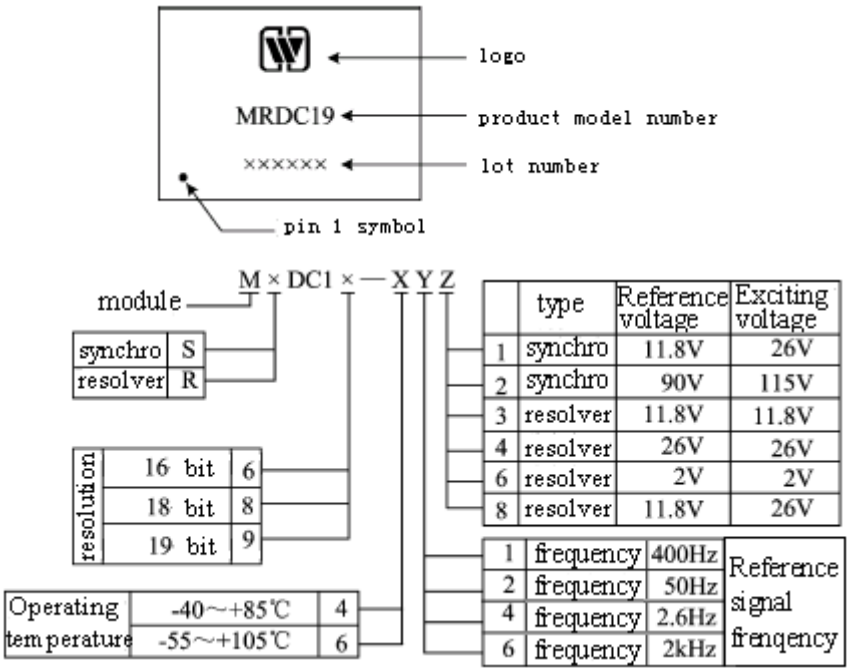

Figure 8 Descriptions of product name

Application notes:

★Polar voltage of power supply should be correct to avoid burn-out.

★While assembling, the bottom of the product should be placed close to the board to avoid damage to the pins. If necessary, take shockproof measures.

★When product is ordered, detailed electrical performance specifications should be referred to corresponding business standard.